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High-Performance Logic Circuits Constructed on Single CdS Nanowires

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ABSTRACT

A high-performance NOT logic gate (inverter) was constructed by combining two identical n-channel metal–semiconductor field-effect transistors (MESFETs) made on a single CdS nanowire (NW). The inverter has a voltage gain as high as 83, which is the highest reported so far for inverters made on one–dimensional nanomaterials. The MESFETs used in the inverter circuit show excellent transistor performance, such as high on/off current ratio (∼10^7), low threshold voltage (∼–0.4 V), and low subthreshold swing (∼60 mV/dec). With the assembly of three identical NW MESFETs, NOR and NAND gates have been constructed.

Introduction. One-dimensional (1D) single-crystalline nanostructures, such as semiconductor nanowires (NWs), nanobelts (NBs), and carbon nanotubes (CNTs), could be of ideal building blocks for nanoelectronic devices.[1−6] These nanostructures present unique advantages over conventional materials, as they enable integration of high-performance device elements onto virtually any substrate.[2,7,8] Field-effect transistors (FETs), which are the basic component of present computer circuitry, have been fabricated with individual NWs, NBs, and CNTs on various substrates.[1−3,7−9] High-κ dielectric top gate,[10−12] surrounding-gate,[13−16] etc., have been employed to improve the performance of the nanoFETs. Their high performance is comparable to or even exceeds bulk materials.[10−11,15,17,18] The next challenge step in the development of integrated nanoelectronics would be the construction of integrated electronic circuits along single CNTs, NWs, or NBs to demonstrate digital logic operation.[1,5−7]

Metal−semiconductor FETs (MESFETs) made on single CdS NBs[4] and ZnO nanorods[19] have shown excellent electrical transport performance. Different from metal−insulator−semiconductor FETs (MISFETs), MESFETs have no gate dielectrics between a Schottky gate and a semiconductor channel, which provides significant capacitive coupling that enables them to have both large voltage and signal power gains.[19] Besides, since no dielectric is needed between the Schottky gate and the semiconductor channel, the fabrication process of integrated electronic circuits based on nanoMESFETs should be much simpler. We have demonstrated that high-performance NB MESFETs[4] and enhancement-mode NW MESFETs can be realized by adopting a top surrounding Schottky gate.[20] Moreover, a top gate can control the nanoFETs individually by modulating the channel conductance of the single NWs/NBs locally, which has an advantage in integrating the FET devices into more complex and functional electronic circuits. In this Letter, we report the construction of a high-performance NOT logic gate (inverter), NOR, and NAND gate on CdS NWs. The basic components of these devices are high-performance MESFETs made on single NWs where top Schottky gates were employed.

Experiment. The CdS NWs used for fabrication of logic gate devices were synthesized and effectively doped with In that acts as a shallow donor via the chemical vapor deposition (CVD) method described previously.[20,21] The CdS NWs have smooth surfaces, and uniform diameters (∼200 nm) along the growth direction. For fabrication of the inverter, two identical MESFETs were made on one single CdS NW. The fabrication processes are as follows: First, CdS NWs were dispersed in ethanol with an ultrasonic process. Then the CdS NW suspension solution was dropped on an oxidized Si substrate, which has a SiO_2 layer of about 600 nm thick on the top. Three In/Au (10/120 nm) ohmic contact electrodes were defined at the two terminals and the middle of a single CdS NW, respectively, with UV lithography followed by thermal evaporation and lift-off processes. The space distance between the neighboring ohmic electrodes is about 20 μm. Finally, two Au Schottky contact electrodes (3 μm wide, 120 nm thick) were made between the three ohmic contact electrodes, respectively, on the CdS NW. The Au electrode fabrication process *is* similar to that mentioned

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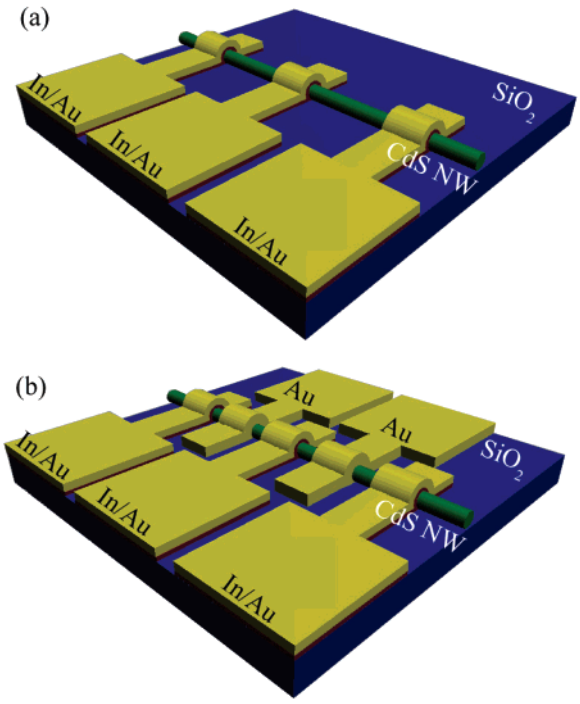

Figure 1. Schematic illustration of the major fabrication process for an inverter made on a single CdS NW. (a) Three ohmic electrodes were first patterned on a single NW which is placed on an oxidized Si substrate. (b) Two Au Schottky contacts were made on the CdS NW to serve as the gate electrodes.

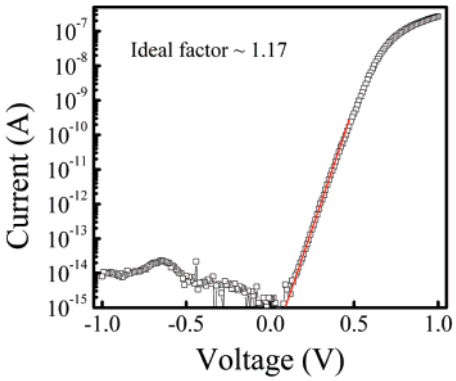

Figure 2. $I-V$ characteristic of the Au/CdS NW Schottky diode together with the fitting result (the straight line).

above. Metals In (with a low work function) and Au (with a high work function) can form ideal ohmic contact and Schottky contact with CdS NW, respectively.[20] Figure 1 shows a schematic illustration of the fabrication process. Room-temperature electrical transport measurements were done with a semiconductor characterization system (Keithley 4200).

Results and Discussion. An Au/CdS NW Schottky diode, as a two-terminal device, is formed between any neighboring Au Schottky contact and In/Au ohmic contact in the inverters made on single CdS NWs. Figure 2 shows $I-V$ characteristic curve of such a Schottky diode. It shows an excellent rectification characteristic with a high on/off current ratio of about 10^7 when the voltage changes from $+1$ to -1 V. The Schottky junction between the Schottky electrode and the NW has an ideal factor of about 1.16 and a barrier height

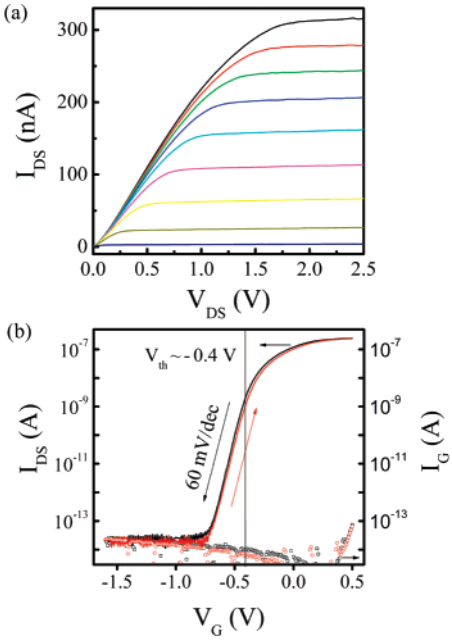

Figure 3. Performance of a single CdS NW MESFET. (a) $I_{DS}-V_{DS}$ curves with V_G changing from 0.5 to -0.5 V, step by 0.125 V. (b) $I_{DS}-V_G$ and I_G-V_G curves measured at $V_{DS} = 1$ V on an exponential scale. The arrows indicate the gate voltage sweeping direction.

of 0.78 V. These values are obtained by fitting the $I-V$ relation of the metal−semiconductor Schottky junction using thermionic emission model, which is expressed as $I = I_0[\exp(qV)/nkT - 1]$, where I_0 is the reverse saturation current given by $I_0 = A^*T^2 \exp(-q\Phi_{Bn}/kT)$, A^* is Richardson's constant (~ 23 A/K^2 cm^2 for CdS), Φ_{Bn} is the barrier height, q is the electronic charge, k is Bolzmann's constant, T is the absolute temperature, and n is the ideal factor. Here, n is quite close to 1, the value of an ideal Schottky junction, and Φ_{Bn} is close to those reported for bulk single-crystal CdS/Au Schottky junctions.[22,23]

Electrical transport measurements on the two identical CdS NW MESFETs in the inverters show they have uniform performance. Figure 3a shows a typical source−drain current (I_{DS}) versus source−drain voltage (V_{DS}) relations of one such nanoMESFET measured at various gate voltages (V_G). For a given V_G, I_{DS} increases linearly with V_{DS} at lower V_{DS} and saturates at higher V_{DS}. Besides, the conductance shows a drastic decrease with increase of applied negative V_G. These behaviors are typical characteristics of an n-channel depletion-mode (D-mode) MESFET.

The gate transfer characteristic with V_G being cycled is presented in Figure 3b. At $V_{SD} = 1$ V, an on−off current ratio larger than 10^7 can be obtained when V_G changes from 0.5 to -1 V. Such an on−off current ratio is on the same order of the highest value for the NW FETs reported so far ($\sim 10^7$ for omega-shaped-gate ZnO NW FETs).[16] The threshold voltage (V_{th}) can be determined to be about -0.4 V from the intersection point of exponential and nonexponential region of the I_{DS}-V_G curve.[24] The I_{DS} decreases exponentially below the threshold voltage (subthreshold region). The subthreshold swing (S) can be obtained to be about 60 mV/dec in the subthreshold region with the equation $S = \ln$

10[dV_G/d(lnI_{SD})]. The obtained S value is approximate to the theoretical limit ($S = (K_BT/q)\ \ln(10) \sim 60$ mV/dec) for MISFETs at room temperature.[22] S is a key parameter for transistors. The smaller the S value is, the easier it is to switch off the transistor, and this is particularly important for low threshold voltage and low-power operation for FETs scaled down to small sizes.[10] In addition, only a very small V_{th} hysteresis (~20 mV) is observed when the gate voltage is cycled (Figure 3b). The transconductance g_m (=dI_{DS}/dV_G) obtained from the $I_{DS}-V_G$ curve has a maximum value of about 0.46 μS. Normalized by the diameter of the NW, a transconductance of 2.3 μS μm^{-1} is obtained. The leakage current (I_G) versus V_G relation is also plotted in Figure 3b. The maximum I_G is about 100 fA, which is smaller than I_{DS} at identical V_G by more than 6 orders of magnitude, confirming the high quality of the Schottky gate for the CdS NW MESFETs. It is worth noting that the gate leakage current is more than 4 orders of magnitude lower than the Schottky forward current at comparable voltages. This is because the drain voltage has changed the electric potential distribution on the Schottky barrier.[24]

In comparison to the performance of the CdS NB MESFETs we reported previously,[4] the on−off current ratio of CdS NW MESFETs here is 1 order of magnitude lower. However, the threshold voltage is about 1 V lower, and threshold voltage hysteresis as well as subthreshold swing hysteresis are smaller. Since the doping concentrations for the NWs and NBs are nearly on the same level, and the off-currents of the NW and NB MESFETs are on the same order of magnitude, the smaller cross section of the NW may result in a smaller on current and therefore a smaller on−off ratio (~10^7). However, the smaller cross section of the NW together with an omega-shaped surrounding top gate geometry results in a stronger gate depletion effect and accordingly a lower threshold voltage. Herein, because the voltage swing of the gate is smaller, the charges stored in the gate/NW interface are less.[12] Therefore, the threshold voltage hysteresis and subthreshold swing hysteresis of the NW MESFETs are smaller.

Figure 4a shows a field emission environmental scanning electron microscope (ESEM) (Quanta 200 FEG) image of the inverter constructed on two high-performance MESFETs made on a single CdS NW. In the circuit of the inverter, one MESFET was used as a switch, and the other was used as a load. For a dc measurement, the power supply V_{DD} (shown in the inset of Figure 4b) is optimized to be 5 V. The transfer characteristic of the inverter with input voltage (V_{IN}) being cycled is shown in Figure 4b. When the V_{IN} is logic 0 (e.g., $V_{IN} = -0.5$ V), the switch transistor is cut off. Then, only the off current of the switch transistor flows through the load transistor. At these low currents, the voltage appearing across the load transistor is very low and the output voltage (V_{OUT}) is close to V_{DD} (logic 1). When the V_{IN} is logic 1 (e.g., $V_{IN} = 0$ V), the switch transistor is on, and the V_{OUT} is close to 0 V (logic 0). Note that in order to realize multistage logic, e.g., driving an identical inverter, the voltage range of V_{OUT} should be shifted by adding a level-shifting diode. To use a logical gate as part of a more complicated

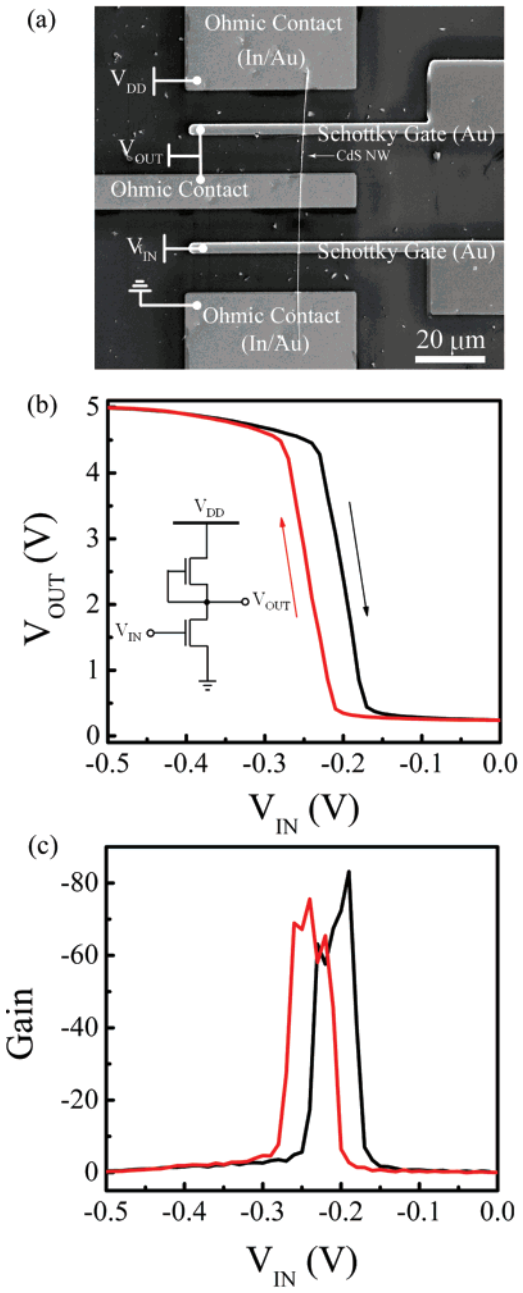

Figure 4. (a) ESEM image of an inverter made on one single CdS NW. (b) Transfer characteristic of the inverter depicted in (a). Inset: the circuit diagram of the inverter. (c) The gain of the inverter vs the input voltage. *A* maximum voltage gain of 83 is obtained.

computing system, a gain ($\Delta V_{OUT}/\Delta V_{IN}$) of at least 1 is required. The most significant characteristic of our inverter is that it exhibits a gain as high as 83 (Figure 4c). To the best of our knowledge, this is the highest reported gain for inverters made on 1D nanomaterials, including carbon nanotubes and semiconductor NWs/NBs. Usually, a high transconductance of the transistors can result in a high gain of an inverter.[10] In our case, the transconductances of the transistors are not very high. We think the reason for the high gain of the inverter may result from the very low channel conductance of the transistor in the saturated region. Qualitatively, the maximum voltage gain should be equal to the transconductance divided by the sum of the channel

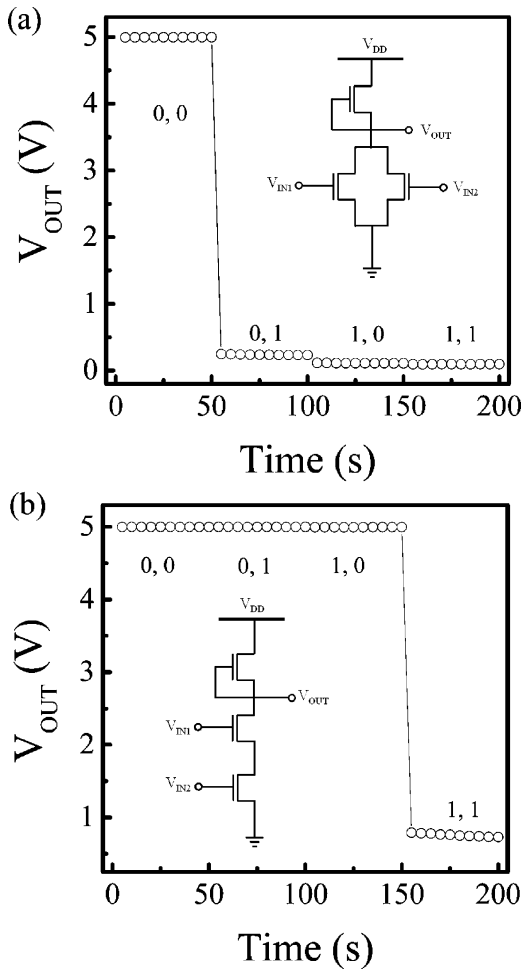

Figure 5. (a) Output voltage of a CdS NW NOR gate for the four possible input states: (0, 0), (0, 1), (1, 0), and (1, 1). Logic input 0 is −0.5 V and logic input 1 is 0 V. Inset: the circuit diagram of the NOR gate. (b) Output voltage of a CdS NW NAND gate for the four possible input states: (0, 0), (0, 1), (1, 0), and (1, 1). Logic input 0 is −0.5 V and logic input 1 is 0 V. Inset: the circuit diagram of the NAND gate.

conductances of the two transistors (essentially connected in parallel). The very low channel conductance overcomes the low transconductance of the transistors. It is expected that through further reducing the gate length and space distance between the source and drain contacts, higher transconductances of the NW MESFETs and accordingly higher gains of the inverters should be obtained.

We have also assembled three identical MESFETs to construct NOR and NAND gates. Two of the MESFETs were constructed on a NW in the same way as that mentioned in fabricating the inverter. The other MESFET was constructed on a NW on another oxidized Si substrate. The electrodes were interconnected via aluminum wires. Figure 5a is the result for a NOR gate, where the switch transistor in the inverter was replaced by two identical MESFETs combined in parallel (as shown in the inset). The V_{OUT} is plotted as a function of the four possible input states (0, 0), (0, 1), (1, 0), and (1, 1) in the figure. When either or both of the inputs are logic 1, at least one of the switch transistors is turned on, resulting in V_{OUT} to be 0 V (logic 0). A logic 1 output state is achieved only when both inputs are logic 0; i.e., both of the switch transistors are cut off. Figure 5b is the result for a NAND gate, where the switch transistor in the inverter was replaced by two identical transistors assembled in series (as shown in the inset). The V_{OUT} is plotted as a function of the four possible input states (0, 0), (0, 1), (1, 0), and (1, 1) in the figure. When either or both of the inputs are logic 0, the V_{OUT} is close to 5 V (logic 1). Low output voltage (logic 0) is achieved only when both inputs are logic 1; i.e., both of the switch transistors are turned on.

Conclusion. In conclusion, based on two or three high-performance identical CdS NW MESFETs, logic circuits, including inverter, NOR and NAND gate were assembled. The D-mode MESFETs made on single CdS NWs show excellent transistor parameters, such as large on−off current ratio ($\sim 10^7$), low threshold voltage (~ -0.4 V), and small subthreshold swing ($\sim$60 mV/dec). The inverters made on single CdS NWs have a voltage gain as high as 83. This is the highest reported gain for the inverters made on 1D nanomaterials so far. Our results demonstrate that high-performance NW MESFETs with a top surrounding gate can be an active candidate of building blocks for assembling functional nanodigital circuits.

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