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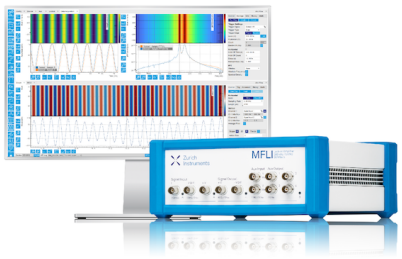

Enhancement-mode metal-semiconductor field-effect transistors based on single *n*-CdS nanowires

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Enhancement-mode (E-mode) metal-semiconductor field-effect transistors (MESFETs) based on single nanowires (NWs) were reported. The single NW used is *n*-CdS NW. Source-drain channel of the nano-MESFET is pinched off by the top surrounding Schottky gate at zero bias. When Schottky gate voltage (V_G) changes from 0 to 0.25 V, the source-drain current increases exponentially with V_G, and an on/off current ratio of 5×10^3 is obtained. The maximum transconductance is 14.6 nA/V, and the gate leakage current is lower than source-drain current by more than two orders of magnitude. Their results suggest a way of fabricating E-mode nano-field-effect transistors. © *2007 American Institute of Physics*. [DOI: 10.1063/1.2710004]

Semiconductor nanostructures such as nanowires (NWs) and nanobelts (NBs) are attractive building blocks for nanoelectronic/photonic devices due to their physical/chemical properties.[1,2] In recent years, there is intense interest in studying nano-field-effect transistors (FETs) based on single NWs and NBs. Up to date, metal-insulator-semiconductor field-effect transistors (MISFETs) in nanoscale based on carbon nanotubes[3–9] and various semiconductor NWs/NBs (Refs. 10–19) have been widely studied. Most reported nano-MISFETs work in the depletion mode (D mode). Enhancement-mode (E-mode) (normally off) FETs, which do not have a conductive channel at zero gate voltage, have more advantage than D-mode FETs in high speed and low power consumption operation devices.[20] However, E-mode FETs are usually more difficult to be implemented. Metal-semiconductor field-effect transistor (MESFET) is another important type of FETs, where the source-drain current is controlled by a Schottky gate. Park *et al.* have fabricated D-mode ZnO nanorod MESFETs (Ref. 21) and we have fabricated D-mode CdS NB MESFETs.[22] We consider that NW/NB MESFETs may also work in the E mode, since if the cross sections of the NWs/NBs are small enough and the gates are well defined, the built-in potential of the Schottky junction might be sufficient to totally deplete the channel region. In this letter, we report the results of fabricating and characterizing E-mode nano-MESFETs based on single *n*-CdS NWs. In contrast to Park *et al.*,[21] who used a predefined back Schottky gate that has a small contact area with ZnO nanorod, we adopted a top surrounding Schottky gate, which has larger contact area with the CdS NW, to increase the gate depletion effect. Such surrounding gate geometry had demonstrated their high performance in nano-MISFETs.[15,17]

The *n*-CdS NWs used in this study were synthesized and effectively doped with indium (In) that acted as shallow donor via the chemical vapor deposition method.[18] In the synthesis process, CdS (99.995%) powders were used as the source, pieces of Si wafers covered with 10 nm thick thermally evaporated Au catalysts were used as the substrates, and a small In (6 *N*) grain was used as the dopant. Prior to heating, a quartz tube inside a tube furnace was cleaned with high-purity argon (Ar) for 90 min. Then under a constant Ar flow [(200 SCCM) (SCCM denotes cubic centimeter per minute at STP)], the furnace was rapidly heated to 800 °C. A quartz boat loaded with the In grain, CdS powders, and Si substrates in sequence was inserted into the quartz tube, with In grain at the upstream of the Ar gas. The distance between In and CdS was about 20 cm and that between CdS and the Si substrates was about 15 cm. The local temperatures for In grain, CdS powders, and Si substrates are about 750, 800, and 720 °C, respectively. The synthesis duration was about 1 h. The synthesized products were characterized by using a field emission scanning electron microscope (FESEM) (AMRAY 1910 FE) and a high-resolution transmission electron microscope (HRTEM) (Tecnai F30).

The single *n*-CdS NW E-mode MESFETs were fabricated as follows. First, the *n*-CdS NW suspension was dropped on oxidized Si substrates with a SiO_2 top layer of about 200 nm thick. Second, UV lithography followed by thermal evaporation and lift-off processes was used to fabricate the source and drain Ohmic contact In/Au electrodes (10/120 nm) at the two terminals of a single *n*-CdS NW. Last, a top surrounding Schottky Au gate electrode (3 μm wide, 120 nm thick) was made across the NW between the source and drain electrodes by the similar process mentioned above. Room-temperature electrical transport measurements on single *n*-CdS NW E-mode MESFETs were done with a semiconductor characterization system (Keithley 4200).

Figure 1(a) shows a typical FESEM image of as-synthesized CdS NWs. The CdS NWs have smooth surfaces and uniform diameters along the growth direction. Figure 1(b) is a TEM image of an as-synthesized CdS NW. We can see that the diameter of the NW is about 180 nm. Figure 1(c) is a HRTEM image of the CdS NW. The corresponding selected area electron diffraction (SAED) pattern recorded along the [0001] zone axis is shown in the inset. The lattice planes with a space distance of about 0.206 nm are seen clearly along the growth direction. According to the data of Ref. 23, these planes can be indexed as $(11\bar{2}0)$ planes. The Miller indices are labeled in the SAED pattern. The HRTEM and SAED results demonstrate that the synthe-

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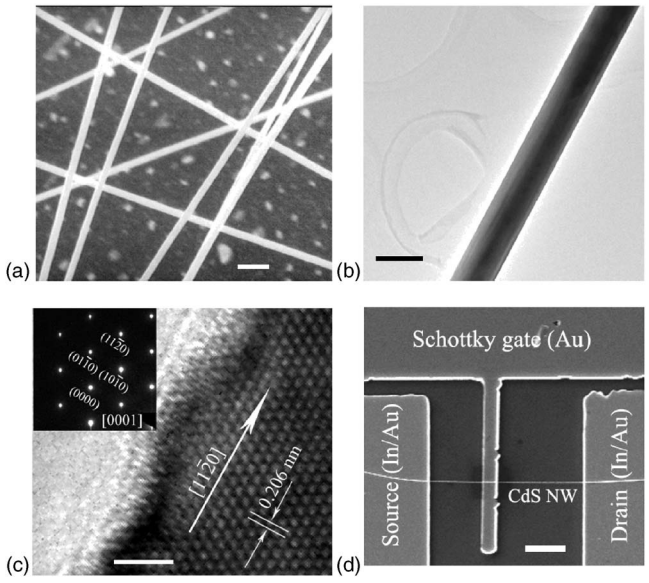

FIG. 1. (a) FESEM image of as-synthesized CdS NWs. Scale bar is 1 μm. (b) TEM image of a single as-synthesized CdS NW. Scale bar is 200 nm. (c) HRTEM image of the CdS NW depicted in (b). Scale bar is 2 nm. The inset is the corresponding SAED pattern recorded along the [0001] zone axis. (d) FESEM image of a single *n*-CdS NW E-mode MESFET. Scale bar is 10 μm.

sized NW is single crystal CdS with the wurtzite structure, and the growth direction is [11$\bar{2}$0].

A FESEM image of a single *n*-CdS NW E-mode MESFET is shown in Fig. 1(d). The diameter of the NW in the device is about 200 nm. The gate length of the device is about 3 μm. The space distance between the source and drain electrodes is about 40 μm. Figure 2 shows several two terminal electrical measurement results. Before evaporating the top Au Schottky gate, the *I-V* curve of the source drain is a straight line, indicating the formation of good Ohmic contacts between the In/Au electrodes and the *n*-CdS NW. From the *I-V* curve and the dimension of the *n*-CdS NW, the resistivity of the *n*-CdS NW obtained is 0.76 Ω cm. After evaporating a Au Schottky gate, the source-drain channel is pinched off. The source-drain current is only about 5×10^{-15} A, when the source-drain bias is 0.4 V. The *I-V* relations between source gate and drain gate, where the source or the drain was grounded, show excellent rectification behavior, which indicates a good Schottky contact between the Au electrode and the *n*-CdS NW. The reverse current for both source gate and drain gate is about 3.1×10^{-5}A cm^{-2} at a gate bias of −0.4 V. On/off current ratios of both the source-gate and drain-gate Schottky junctions are greater than 10^4 when the gate bias changes from −0.4 to +0.4 V.

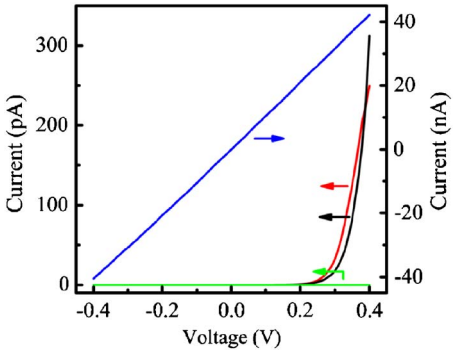

FIG. 2. (Color online) Two-terminal *I-V* curves. The green and blue ones are the *I-V* curves of a single CdS NW between two In/Au contacts with and without a top Au contact, respectively. The black and red ones are the *I-V* curves measured between source gate and drain gate, where the source and the drain were grounded, respectively.

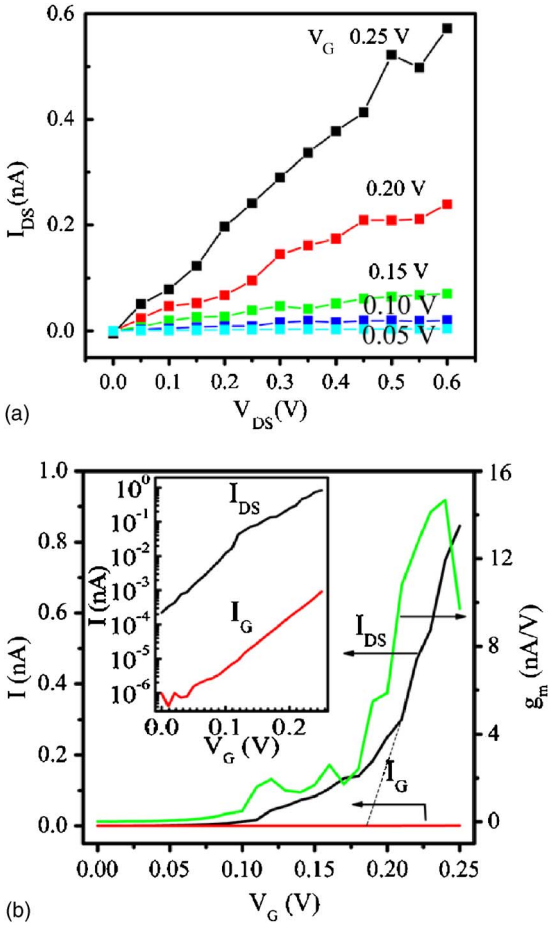

FIG. 3. (Color online) (a) I_{DS}-V_{DS} curves with V_G changing from 0.05 to 0.25 V, step by 0.05 V. (b) The I_{DS}-V_G (black), I_G-V_G (red), and g_m-V_G (green) curves (V_{DS}=0.6 V). Inset: I_{DS}-V_G and I_G-V_G curves on an exponential scale.

Figure 3(a) shows the source-drain current (I_{DS}) versus source-drain voltage (V_{DS}) relations at various gate voltages (V_G). The source electrode was grounded. We can see that the I_{DS} increases with V_{DS} for a given V_G, and the conductance shows a drastic increase with positive V_G. The I_{DS} vs V_G and I_G vs V_G relations measured at V_{DS}=0.6 V are shown in Fig. 3(b). In our experiment, the forward V_G is limited to be lower than 0.25 V to avoid excessive gate leakage current (I_G). The threshold voltage (V_{th}) can be determined to be about −0.18 V by extrapolating the linear region. The transconductance (g_m=dI_{DS}/dV_G) vs V_G relation is also plotted in this figure, from which a zero transconductance is obtained at V_G=0 V, and a maximum transconductance of about 14.6 nA/V is obtained at V_G=0.24 V. All the above results show clearly that this device is an E-mode MESFET. The inset of Fig. 3(b) shows the I_{DS}-V_G curve together with the I_G-V_G curve on an exponential scale. We can see that when the gate voltage changes from 0 to 0.25 V, the I_{DS} increases exponentially with V_G. An on/off current ratio can be obtained to be about 5×10^3 when V_G changes from 0 to 0.25 V. Besides, the I_G is about two orders of magni-

tude lower than the I_{DS}. We attribute the realization of the n-CdS NW E-mode MESFET to (1) the NWs with appropriate doping concentration and metal electrodes with proper work function used, which ensure the formation of ideal Schottky and Ohmic contacts in the device; and (2) the surrounding top Schottky gate geometry adopted, which has formed an effective built-in potential that is sufficient to totally deplete the source-drain channel.

In conclusion, E-mode nano-MESFETs based on single NWs were reported. A top surrounding Au Schottky contact gate geometry was adopted. The fabricated E-mode nano-MESFETs have a zero transconductance at $V_G=0$ V, a maximum transconductance of about 14.6 nA/V, and a threshold voltage of about 0.18 V. The gate leakage current is lower than source-drain current by more than two orders of magnitude when V_G is lower than 0.25 V. Our results demonstrate that nano-MESFETs based on single NWs can be designed to work in the E mode. The development of E-mode nano-MESFETs based on single NWs/NBs may enhance the versatility of NW/NB device technologies and extend their application domain.

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