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Back-gate ZnO nanowire field-effect transistors each with a top Ω shaped Au contact

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We have fabricated depletion and enhancement modes (D-mode and E-mode) back-gate metal-insulator-semiconductor field-effect-transistors (MISFETs), using two kinds of ZnO nanowires (NWs) labeled as A and B, respectively. The NWs A and B were synthesized via the vapor phase transport method with ZnO/C admixture and Zn as the sources, respectively. Each of the MISFETs has a top Ω shaped Au contact on the conductive channel. Compared to that without any top Au contact, the on/off ratio ($\sim 10^6$) of the ZnO NW A MISFET increases by a factor of 10^3, and is the highest one among the back-gate ZnO NW MISFETs ever reported; while the ZnO NW B MISFET changes from D-mode to E-mode when a top Au contact is added. The effects of the Au/ZnO NW contacts on the performances of the NW A and B MISFETs were discussed. © *2008 American Institute of Physics*. [DOI: 10.1063/1.2959075]

Semiconductor nanowires (NWs) and nanobelts (NBs) are attractive building blocks for nanoelectronic/photonic devices due to their remarkable physical/chemical properties.[1,2] Up to date, various NW/NB metal-insulator-semiconductor field-effect-transistors (MISFETs) have been fabricated.[3–5] Most reported NW/NB MISFETs work in the depletion-mode (D-mode). Enhancement-mode (E-mode) (normally off) MISFETs have advantage in high speed and low power consumption operation devices.[6] ZnO has attracted considerable attention over the last few years.[7] Various D-mode ZnO NW MISFETs have been fabricated.[8–10] Recently Hong *et al.* reported the E-mode back-gate ZnO NW MISFET, in which the ZnO NW was passivated by poly(methyl methacrylate).[11]

In this letter, we studied back-gate ZnO NW MISFET with a top Ω shaped Au contact. Two kinds of ZnO NWs (labeled as A and B), which were synthesized with different sources, were used. The MISFETs based on single NW A and B work in D-mode and E-mode, respectively. Back-gate ZnO NW MISFETs without any top Au contact were also fabricated for comparison.

The two kinds of ZnO NWs were synthesized via the vapor phase transport method.[12] For the ZnO NW A, the source was the mixture of ZnO (99.99%) and C (99.9%) (with mass ratio of 1:1). For the ZnO NW B, the source was metal Zn (99.9%). The products were characterized using a field emission scanning electron microscope (FESEM), and a high-resolution transmission electron microscope (HRTEM). The single ZnO NW MISFETs (with or without any top Au contact) were fabricated on p^+-Si substrates with a 300 nm thick SiO_2. The source and drain Ohmic contact are In/Au (10/100 nm) electrodes. The top surrounding (Ω shaped) Au contact is 5 μm wide, 100 nm thick. The channel length of the ZnO NW MISFETs with and without top Au contacts is 40 and 4 μm, respectively. The p^+-Si substrate is used as the back gate. The process details are presented in Ref. 4. Tens of the devices were fabricated. Room-temperature electrical transport measurements were done with a semiconductor characterization system (Keithley 4200).

Figure 1(a) shows a typical FESEM image of the ZnO NW (A or B). The NWs are around 200 nm in diameter and tens of microns in length. Typical HRTEM image [Fig. 1(b)] together with the corresponding selected area electron diffraction (SAED) pattern recorded along the $[1\bar{2}10]$ zone axis (the inset) show that both NWs A and B are single crystalline wurtzite structure and their growth direction is [0001].

The electrical transport measurement results (the source electrodes were grounded) on single ZnO NW A and B MISFETs without any top Au contact are shown in Figs. 2(a) and 2(b), respectively. The linear relation of the source-drain current and voltage (I_{sd}-V_{sd}) for both ZnO NW A and B MISFETs suggests that the In/Au electrodes have formed good Ohmic contacts with both the ZnO NWs A and B. The obtained resistivities for NWs A and B are about 0.5 and 28.5 Ω cm, respectively. The insets of Figs. 2(a) and 2(b) show the I_{sd} versus gate voltage (V_g) (V_{sd}=1 V) relations in semilog scale, respectively. In both cases, the I_{sd} increases with the positive V_g, indicating the *n*-type conductive channel. For ZnO NW A MISFET, we can obtain the threshold voltage (V_{th}), the transconductance ($g_m = dI_{sd}/dV_g$), the on/off ratio, and the off-state current to be about −44 V, 24 nS,

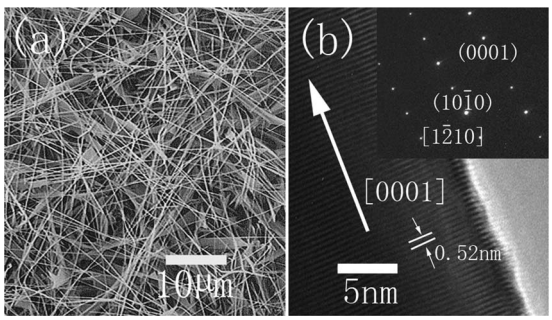

FIG. 1. (a) Typical FESEM image of the ZnO NWs. (b) Typical HRTEM image of the NW. The arrow highlights the growth direction of [0001]. The inset is the corresponding SAED pattern recorded along the $[1\bar{2}10]$ zone axis.

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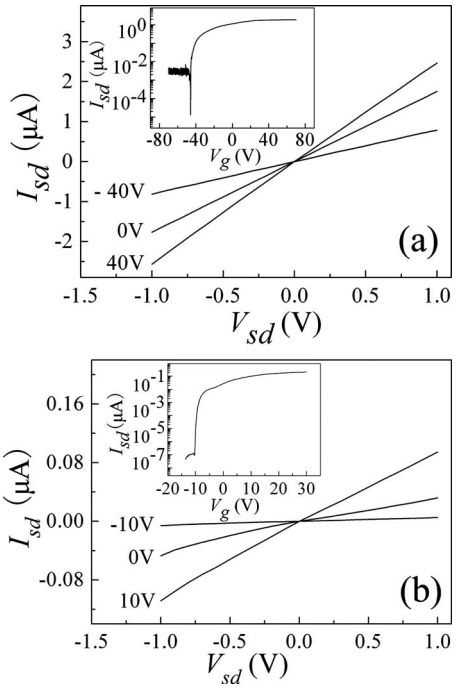

FIG. 2. (a) I_{sd}-V_{sd} curves measured at various back-gate voltage V_g for a ZnO NW A MISFET without any Au contact. The inset shows the semilog plot of I_{sd}-V_g curve measured at V_{sd}=1 V. (b) I_{sd}-V_{sd} curves measured at various V_g for a ZnO NW B MISFET without any Au contact. The inset shows the semilog plot of I_{sd}-V_g curve measured at V_{sd}=1 V.

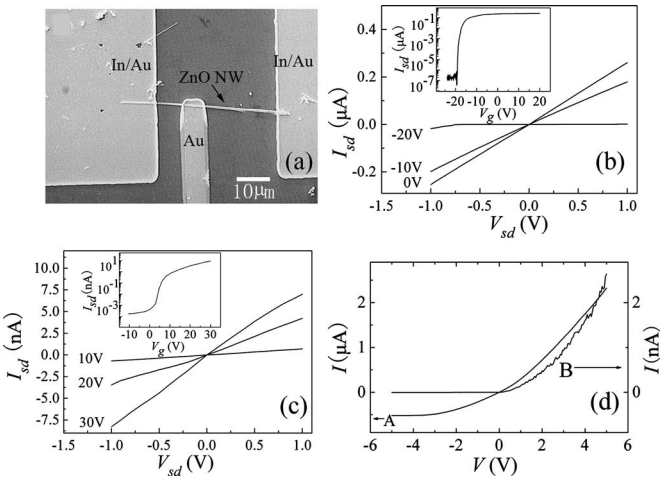

FIG. 3. (a) FESEM image for a ZnO NW MISFET with a top Au contact. (b) I_{sd}-V_{sd} curves measured at various V_g for a ZnO NW A MISFET with a top Au contact. The inset shows the semilog plot of I_{sd}-V_g curve measured at V_{sd}=1 V; (c) I_{sd}-V_{sd} curves measured at various V_g for a ZnO NW B MISFET with a top Au contact. The inset shows the semilog plot of I_{sd}-V_g curve measured at V_{sd}=1 V; (d) *I-V* curves between an In/Au electrode and the top Au electrode for the ZnO NW A and B, respectively.

5×10^2, and 3×10^{-9} A, respectively. The electron mobility (μ) and the electron concentration (n) of the ZnO NW A can be estimated to be about 7.9 $cm^2/V\,s$ and 1.1×10^{18} cm^{-3}, respectively, from the equations $\mu=g_m\times L\times\ln(2t/r)/(2\pi\varepsilon_0\varepsilon\times V_{sd})$,[13] and $\rho=1/(e\times n\times\mu)$, where t and ε are the thickness and the relative dielectric constant of SiO_2(=3.9), respectively, L is the channel length (4 μm), and r is the radius of the NW. For ZnO NW B MISFET, we can obtain the V_{th}, g_m, the on/off ratio, and the off-state current to be about −9.5 V, 5.6 nS, 10^6, and 1×10^{-13} A, respectively. The on/off ratio value is the highest one among the reported back-gate ZnO NW MISFETs, indicating the high quality of ZnO NW B. The μ and n values of the ZnO NW B are estimated to be about 2 $cm^2/V\,s$ and 1.0×10^{17} cm^{-3}, respectively. It has been suggested that oxygen vacancies and zinc interstitials can serve as shallow donors in ZnO.[14,15] In our case, we think there are more oxygen vacancies and zinc interstitials in ZnO NWs A, due to the existence of the reducing agent (Carbon) during the synthesis process, which may account for the higher electron concentration in ZnO NWs A.

The electrical transport measurement results on single ZnO NW A and B MISFETs each with a top Au contact [corresponding FESEM image is shown in Fig. 3(a)] are shown in Figs. 3(b) and 3(c), respectively. The insets of them are the semilog plots of I_{sd}-V_g (V_{sd}=1 V) curves, respectively. After adding the top Ω shaped Au contact, the V_{th} of the ZnO NW A MISFET reduces to −17 V. The on/off ratio of it increases to 10^6. This value is the highest one among the reported back-gate ZnO NW MISFETs. After fabricating a top Ω shaped Au contact, the V_{th} of the ZnO NW B MISFET changes to +6 V. The positive V_{th} value means that the n-channel NW B MISFET is E-mode. Its on/off ratio is 5×10^4. The off-state currents of the both NW A and B MISFETs are around 10^{-13} A.

We have measured the *I-V* curve between the In/Au Ohmic contact electrode and the top Au electrode (the In/Au Ohmic contact electrode was grounded). The results are shown in Fig. 3(d). For NW A, there is only a weak asymmetrical behavior in the *I-V* curve. This indicates that the Au/NW A contact is between Ohmic and Schottky contact behaviors. For NW B, the *I-V* curve exhibits an excellent rectification characteristic. No significant current breakdown is observed at reverse voltage up to −5 V. A forward-to-reverse current ratio is about 10^3 (4/−4 V). This indicates the Au/NW B contact is a Schottky contact.

We think that the reason for the shifts of the threshold voltages of ZnO NW A and B MISFETs is similar to that in our previous work.[4,16] A top surrounding Au contact helps to deplete or narrow the ZnO NW conductive channel, and hence reduces the threshold voltage of the back-gate ZnO NW MISFET. Supposing a typical Schottky contact consisting of a ZnO film and a Au film, we can estimate the width of the depletion layer (W_d) in the ZnO film to be about 100 nm by the equation $W_d=[2\varepsilon_0\varepsilon_s(\varphi_m-\chi_s)/(en)]^{1/2}$,[17] where ε_s, χ_s, and n are the relative dielectric constant (~7.9), the electron affinity (~4.1), and the electron concentration (~1.0×10^{17} cm^{-3} for NW B) of ZnO, respectively, and φ_m, is the work function of Au (~5.3 eV).[18] Thus we think that the 200 nm thick NW B is completely depleted by the top Ω shaped Au Schottky contact, and accordingly the NW B MISFET is E-mode.

It is well known that the chemisorption process at oxygen vacancies at the surface of ZnO NW may reduce the on/off ratio of the ZnO NW FETs. Various dielectric films, such as polyimide, Si_3N_4 and Al_2O_3, were used to passivate the ZnO NW surfaces to increase the on/off ratio.[10,13,19] Herein, we think the enhanced on/off ratio (from 10^3 to 10^6) for the NW A MISFET after fabricating a layer of Au contact may also be due to a passivation effect that reduces the chemisorption process of oxygen vacancies at ZnO NW surface, and causes the off-state current to reduce from

10^{-9} to $\sim 10^{-13}$ A (the measurement limit). On the other hand, we think the quite low off-state current ($\sim 10^{-13}$ A) for the NW B MISFET prior to fabricating a top Au contact reflects that there are fewer oxygen vacancies at the NW B surface, which also agrees with the forementioned conclusion.

In summary, we have fabricated D-mode and E-mode ZnO NW back-gate MISFETs each with a top Ω shaped Au contact on the conductive channel, using two kinds of ZnO NWs (A and B), respectively. Compared to that without a top Au contact, the on/off ratio ($\sim 10^6$) of ZnO NW A MISFET increases by a factor of 10^3, and is the highest reported value among the back-gate ZnO NW MISFETs. While the ZnO NW B MISFET changes from D-mode to E-mode when a top Au contact is added. The effects of the Ω shaped Au/ZnO NW contacts on the NW A and B device performances are discussed, respectively.

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[1]J. T. Hu, T. W. Odom, and C. M. Lieber, Acc. Chem. Res. **32**, 435 (1999).
[2]Z. W. Pan, Z. R. Dai, and Z. L. Wang, Science **291**, 1947 (2001).
[3]W. Park, J. S. Kim, G. C. Yi, and H. Lee, J. Adv. Mater. **17**, 1393 (2005).
[4]R. M. Ma, L. Dai, and G. G. Qin, Nano Lett. **7**, 868 (2007).
[5]R. M. Ma, L. Dai, H. B. Huo, W. J. Xu, and G. G. Qin, Nano Lett. **7**, 3300 (2007).
[6]S. M. Sze, *Physics of Semiconductor Devices* (Wiley, New York, 1981), p. 322.
[7]U. Ozgur, Y. I. Alivov, C. Liu, A. Teke, M. A. Reshchikov, S. Dogan, V. Avrutin, S. J. Cho, and H. Morkoc, J. Appl. Phys. **98**, 041301 (2005).
[8]Y. W. Heo, L. C. Tien, Y. Kwon, D. P. Norton, S. J. Pearton, B. S. Kang, and F. Ren, Appl. Phys. Lett. **85**, 2274 (2004).
[9]Y. Chen, P. Xiong, L. Fields, J. P. Zheng, R. S. Yang, and Z. L. Wang, Appl. Phys. Lett. **89**, 093114 (2006).
[10]K. Keem, D. Y. Jeong, S. Kim, M. S. Lee, I. S. Yeo, U. I. Chung, and J. T. Moon, Nano Lett. **6**, 1454 (2006).
[11]W. K. Hong, D. K. Hwang, K. Park, G. Jo, S. Song, S. J. Park, T. Lee, B. J. Kim, and E. A. Stach, Appl. Phys. Lett. **90**, 243103 (2007).
[12]W. Q. Yang, H. B. Huo, L. Dai, R. M. Ma, S. F. Liu, G. Z. Ran, B. Shen, C. L. Lin, and G. G. Qin, Nanotechnology **17**, 4858 (2006).
[13]W. Park, J. S. Dim, G. C. Yi, M. H. Bae, and H. Lee, Appl. Phys. Lett. **85**, 5052 (2004).
[14]D. C. Reynolds, D. C. Look, B. Jogai, C. W. Litton, T. C. Collins, W. Harsch, and G. Cantwell, Phys. Rev. B **57**, 12151 (1998).
[15]D. C. Look and J. W. Jemsky, Phys. Rev. Lett. **82**, 2552 (1999).
[16]R. M. Ma, L. Dai, and G. G. Qin, Appl. Phys. Lett. **90**, 093109 (2007).
[17]S. M. Sze, *Physics of Semiconductor Devices* (Wiley, New York, 1981), p. 248.
[18]B. J. Coppa, R. F. Davis, and R. J. Nemanich, Appl. Phys. Lett. **82**, 400 (2003).
[19]P. C. Chang, Z. Fan, C. J. Chien, D. Stichtenoth, C. Ronning, and J. G. Lu, Appl. Phys. Lett. **89**, 133113 (2006).