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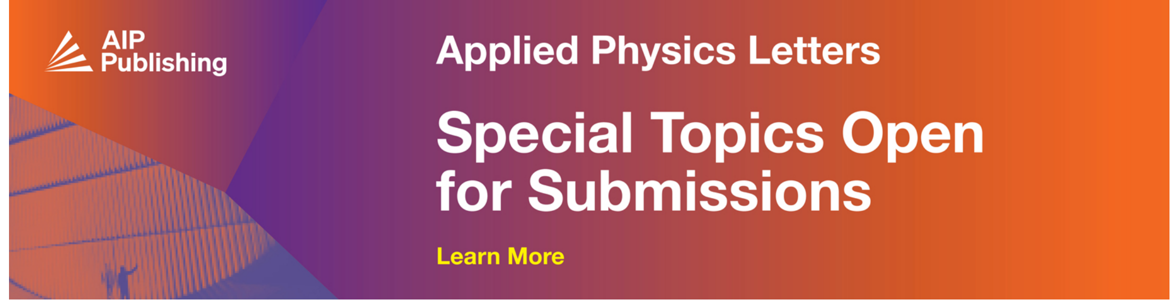

High-performance nanowire complementary metal-semiconductor inverters

R. M. Ma, L. Dai,[a] C. Liu, W. J. Xu, and G. G. Qin[b]
School of Physics and State Key Laboratory for Mesoscopic Physics, Peking University, Beijing 100871, People's Republic of China

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We demonstrated the construction of complementary metal-semiconductor (CMES) inverters with single *n*- and *p*-type nanowires (NWs) on the same chip. A single *p*-type NW was assembled by the side of an *n*-type NW via the electric field assembly method. *n*- and *p*-channel metal-semiconductor field-effect transistors were fabricated with *n*- and *p*-type NWs, respectively. Based on this, high-performance NW CMES NOT logic gate (inverter) was built. The NW CMES inverters have low operating voltage ($\leq$2 V), high voltage gain ($\geq$7), and low static power dissipation ($\leq$0.3 nW). © *2008 American Institute of Physics*. [DOI: 10.1063/1.2967725]

With the development of rational and predictable assembly technology[1–10] and the control of electrical properties during the synthesis processes,[11–19] one-dimensional single-crystalline semiconductor nanowires (NWs) have shown their unique virtues as the building block for constructing powerful future electronic devices. Using bottom-up method, high-performance field-effect transistors (FETs) have been fabricated with NWs on a variety of substrates.[5,8,9,15,20–23] Further, the NW FETs have been used to construct logic circuits. Up to date, *n*-channel metal-oxide-semiconductor and *n*-channel metal-semiconductor logic gates have been fabricated with single NWs.[21,24] Power consumption is an increasingly important issue in general purpose processors. As transistors become smaller and faster, static power dissipation will increase significantly. Complementary logic gates involving both *n*- and *p*-channel transistors have a key characteristic of low static power dissipation, which is especially superior for ever denser circuit integration. So far, in the area of nanoelectronics, complementary metal-oxide-semiconductor (CMOS) inverters have been fabricated with carbon nanotubes[25,26] and NWs.[5,27–29] In this paper, we demonstrated the construction of high-performance complementary metal-semiconductor (CMES) inverters with single *n*- and *p*-type NWs on the same chip.

The *n*- and *p*-type NWs used here are *n*-CdS and *p*-Zn_3P_2, respectively. They were synthesized via the chemical vapor deposition method.[17,30] The formation mechanism of both *n*-CdS and *p*-Zn_3P_2 NWs is based on the well-known vapor-liquid-solid process[31] with Au as the catalyst. The fabrication processes of NW CMES inverters are as follows. First, the *n*-CdS NW suspension solution was dropped on an oxidized p^+-Si substrate, which had a SiO_2 layer of about 600 nm thick on the top. Second, In/Au (20/100 nm) Ohmic contact electrodes were defined at the two terminals of one single *n*-CdS NW via UV lithography, followed by thermal evaporation and lift-off process. A pair of In/Au electrodes was patterned by the side of the *n*-CdS NW, simultaneously. Third, a *p*-Zn_3P_2 NW was assembled between the In/Au electrodes via the electric field assembly method.[2,6] Fourth, three Au (100 nm thick) electrodes were defined with a similar process mentioned above. Two of them were patterned at the two terminals of *p*-Zn_3P_2 NW as Ohmic contact electrodes. The other one was patterned in the middle of the *n*-CdS NW as the Schottky gate (3 μm wide). Finally, an Al electrode (3 μm wide, 100 nm thick) was made in the middle of the *p*-Zn_3P_2 NW as a Schottky gate. Figures 1(a)–1(d) show a schematic illustration of the fabrication process. In order to construct a CMES inverter, the electrodes were interconnected via aluminum wires. The circuit is shown in Fig. 1(d). Room-temperature electrical transport measurements were done with a semiconductor characterization system (Keithley 4200).

Figure 2(a) shows a scanning electron microscope (SEM) image of a CMES inverter, which consists of a *p*-Zn_3P_2 NW metal-semiconductor field-effect transistor (MESFET) and a *n*-CdS NW MESFET. The channel lengths between the source and drain electrodes for *n*- and *p*-MESFETs are 16 and 12 μm, respectively. In the *p*-Zn_3P_2 NW MESFET (right side), the diameter, hole concentration, and mobility of the *p*-Zn_3P_2 NW are about 180 nm, 5×10^{16} cm^{-3}, and 42 cm^2 V^{-1} s^{-1}, respectively. In the *n*-CdS NW MESFET (left side), the diameter, electron concentration, and mobility of the *n*-CdS NW are about 300 nm, 5×10^{16} cm^{-3}, and 300 cm^2 V^{-1} s^{-1}, respectively. Herein, the

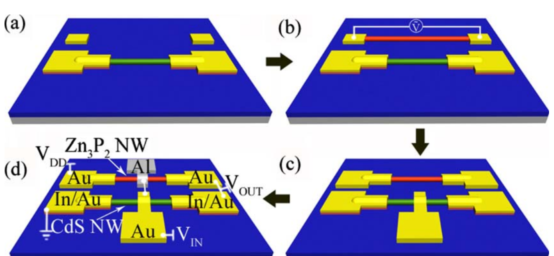

FIG. 1. (Color online) Schematic illustration of the major fabrication process for a CMES inverter made on single *n*-CdS NW and *p*-Zn_3P_2 NW. (a) In/Au Ohmic contact electrodes were defined at the two terminals of one single *n*-CdS NW, and a pair of electrodes was patterned by the side of the *n*-CdS NW, simultaneously. (b) One *p*-Zn_3P_2 NW was assembled between the electrodes pair by the side of the *n*-CdS NW via an electric field assembly method. (c) Three Au electrodes were defined. Two of them were patterned at the two terminals of the *p*-Zn_3P_2 NW as Ohmic contact electrodes. The other one was the patterned in the middle of the *n*-CdS NW as a Schottky gate. (d) An Al electrode was made in the middle of the *p*-Zn_3P_2 NW as a Schottky gate. The circuit of the CMES inverter was also plotted in this figure.

[a]Author to whom correspondence should be addressed. Electronic mail: lundai@pku.edu.cn.
[b]Electronic mail: qingg@pku.edu.cn.

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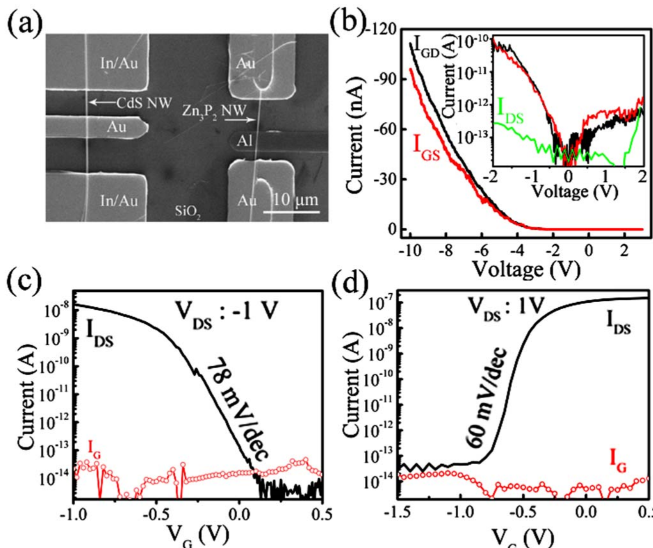

FIG. 2. (Color online) (a) A SEM image of a CMES inverter made with single n-CdS NW and p-Zn_3P_2 NW. (b) Two-terminal I-V curves of the p-MESFET. The black and red ones are the I-V curves measured between drain-gate and source-gate, respectively. Inset: magnified drain-gate, source-gate, and source-drain (green line) I-V curves on an exponential scale. [(c) and (d)] I_{DS}-V_G and I_G-V_G curves for the p-Zn_3P_2 and n-CdS NW MESFETs, respectively.

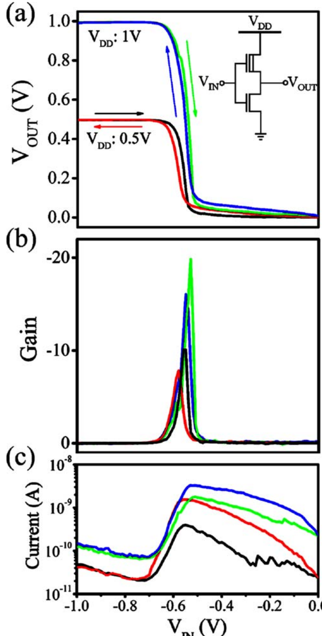

FIG. 3. (Color online) Performances of the NW CMES inverter depicted in Fig. 2(a). (a) Transfer characteristics of the CMES inverter with V_{DD}=0.5, 1 V. Inset: the circuit of the NW CMES inverter. (b) The gains of the inverter. (c) The currents flowing into the inverter. In these figures, the lines in same color are measured simultaneously.

carrier concentrations and mobilities of n- and p-NWs were estimated by fabricating back-gate single NW metal-oxide-semiconductor FETs (MOSFETs) and by analyzing their transport characterization.[17,30] Figure 2(b) shows several two-terminal electrical measurement results of p-MESFETs. The I-V relations between source-gate and drain-gate, where the source or the drain was grounded, show rectification behavior, which indicates a good Schottky contact between the Al electrode and the p-Zn_3P_2 NW. The corresponding magnified I-V curves in the voltage range from −2 to 2 V on an exponential scale are plotted in the inset of Fig. 2(b). The built-in potential of the Al Schottky contact is sufficient to totally deplete the channel region, and the source-drain channel is pinched off (green line in the inset), which enable the p-MESFETs to work in an enhancement mode (E-mode). The turn-on voltage of the Al/p-Zn_3P_2 NW Schottky diode is as high as about −4 V. Such a high turn-on voltage is crucial for the realization of p-MESFETs and CMES inverter depicted below with very low gate leakage current.

The gate transfer characteristic for the p-Zn_3P_2 NW MESFET is presented in Fig. 2(c). The p-Zn_3P_2 NW MESFET exhibits p-channel E-mode characteristic and has a high on/off current ratio of about 5×10^6 and a small maximum gate leakage current (I_G) of about 50 fA in the gate voltage swing region. The gate transfer characteristic for the n-CdS NW MESFET is presented in Fig. 2(d). The CdS NW MESFET exhibits n-channel depletion mode (D-mode) characteristic and has also a high on/off current ratio of about 5×10^6 and a small maximum I_G of about 20 fA in the gate voltage swing region. The threshold voltages (V_{th}) of n- and p-MESFETs can be determined to be about −0.3 and −0.5 V, respectively, from the intersection points of exponential and nonexponential regions of the I_{DS}-V_{G} curves.[20] Note that n-CdS NWs used in this work have diameters of about 300 nm, and the built-in potential of the Schottky junction is not sufficient to totally deplete the channel region without gate voltage. Hence, the n-MESFET works in D-mode and has a negative threshold voltage. Smaller diameters or lower doping concentrations of n-CdS NWs could make the n-CdS NW MESFETs work in E-mode and have positive threshold voltages.[32] This will lower the operating voltage of the CMES inverter further. The I_{DS} decreases exponentially below the threshold voltage (subthreshold region). The subthreshold swing (S) can be obtained to be about 60 and 78 mV/decade for n- and p-MESFETs, respectively, in the subthreshold region with the equation $S=\ln 10[dV_{\mathrm{G}}/d(\ln I_{\mathrm{SD}})]$. The obtained S values for both n- and p-MESFETs are close to the theoretical limit $[S=(K_BT/q)\ln(10)\sim60\ \mathrm{mV/decade}]$ for MOSFET at room temperature.[33] S is a key parameter for transistors. The smaller the S value is, the easier it is to switch the transistor off, and this is particularly important for low threshold voltage and low-power operation for FETs scaled down to small sizes.[34] All the above results suggest that the Al and Au electrodes have acted as excellent Schottky contact gates for the p- and n-channel MESFETs, respectively. Note that the low threshold voltages and small S values can enable the CMES inverter constructed on the n- and p-MESFETs to work at a low operating voltage.

The transfer characteristics of the CMES inverter (supply voltages V_{DD}=0.5, 1 V) with input voltage (V_{IN}) being cycled are shown in Fig. 3(a). We can see sharp switching output swings, which correspond to large gains $(=|dV_{\mathrm{out}}/dV_{\mathrm{in}}|)$ of ∼20 at V_{DD}=1 V and of ∼10 at V_{DD}=0.5 V [Fig. 3(b)]. The key advantage of a complementary inverter is that it consumes low static power since only a small current flows from the V_{DD} to the ground, whether the input is low (the n-FET is off) or high (the p-FET is off). The currents flowing into the NW CMES inverter are shown in Fig. 3(c). We can see that the static currents (when V_{IN}=0 V or V_{IN}=−1 V) are only about 0.3 nA at V_{DD}=1 V

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and about 50 pA at $V_{DD}=0.5$ V. Thus, the static power dissipations are only about 0.3 nW and 25 pW for $V_{DD}=1$ and 0.5 V, respectively.

In conclusion, we have constructed high-performance CMES inverters with single *n*- and *p*-type NWs on the same chip. The key features of our approach include (1) a single *p*-type NW assembled by the side of a single *n*-type NW via the electric field assembly method. The MESFETs made on such *n*- and *p*-type NWs show excellent transistor parameters. (2) Based on the high-performance *n*- and *p*-MESFETs, the CMES inverters with excellent transfer characteristics, such as low operating voltage, high voltage gain, and ultralow static power dissipation, are demonstrated. Compared to the NW CMOS technology, the NW CMES technology has a much simpler fabrication process and lower cost since there is no need for gate dielectrics.

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