Logic gates constructed on CdS nanobelt field-effect transistors with high-κ HfO_2 top-gate dielectrics

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A high-performance NOT logic gate (inverter) was constructed by combining two identical metal-insulator-semiconductor field-effect transistors (MISFETs) made on an individual CdS nanobelt (NB). The MISFETs, which used high-κ HfO_2 dielectrics as the top-gate insulator layer, show excellent performance, such as low threshold voltage (~ -0.1 V), a high on/off ratio ($\sim 10^8$), small subthreshold swing ($\sim$65 mV dec^{-1}) and threshold voltage hysteresis ($\sim$30 mV). The supply voltage for the inverter can be as low as 1 V with a voltage gain as high as 14. When the supply voltage is 7 V, the voltage gain is 72, which is the best reported value, as far as we know, for the inverters based on NB/NW *n*-channel MISFETs. Besides, the inverter can work in a larger input range with highly stable output voltages. Their high output voltages can make full use of the supply voltages, and their low output voltages can be close to zero. NAND and NOR logic gates have been constructed by assembling three such CdS NB MISFETs, which show high performances as well. The operating principle of the inverter is discussed in detail.

Introduction

With controllable morphologies and electrical properties during the synthesis process,[1–7] semiconductor nanowires (NWs) and nanobelts (NBs) have shown their unique virtues as building blocks for nanodevices. Various high-performance devices based on NWs/NBs have been fabricated on a variety of substrates, including plastic substrates, with the bottom-up method.[8–12] The next challenge in the development of integrated nanoelectronics would be the construction of logic gates, which are the basic elements in integrated circuits.[13–15]

CdS NBs/NWs have demonstrated a wide range of device applications, such as laser diodes,[16] photoconductors,[17] field-effect transistors (FETs),[10] piezoelectric nanogenerators,[18] *etc.* Recently, Ma *et al.* reported high-performance logic gates based on CdS NW metal-semiconductor field-effect transistors (MESFETs).[19] However, MESFETs have the demerit of a lower upper limit (<1 V) of on-state gate voltage. In this study, we report the construction of high-performance NOT (inverters), NAND, and NOR gates based on the high-performance CdS NB metal-insulator-semiconductor field-effect transistors (MISFETs) with high-κ HfO_2 top-gate dielectrics. The as-constructed inverters can work reliably when the inputs sweep from -5 to +5 V, exhibiting a much larger input range than that of the inverters based on the CdS NW MESFETs. When the supply voltage (V_{DD}) is 7 V, the voltage gain is about 72, which is the best reported value so far for the inverter based on NB/NW *n*-channel MISFETs. Besides, the high output voltage V_{OH} is quite close to the supply voltage, while the low output voltage V_{OL} is very close to zero. The operating principle of the inverter is discussed in detail.

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Experiments

The *n*-CdS NBs used for the fabrication of logic gate devices were synthesized *via* an improved atmospheric vapor–liquid–solid (VLS) method. The VLS method is widely used for its simple process,[20,21] and high quality crystal NWs or NBs are easily achieved due to the high temperature process. However, the common VLS process for synthesizing CdS nanostructures, where only CdS powders are used as the source, usually leads to CdS nanostuctures with diverse morphologies on the same substrate (as shown in Fig. 1a). This will cause extra difficulty in the later device fabrications. In this work, we synthesized high-quality CdS NWs or NBs with uniform morphology on the same substrate by adding a tiny cadmium (Cd) grain to the CdS source during the VLS process. Pieces of Si wafers covered with 5 nm thick thermally evaporated Au film were used as the substrates. Prior to heating, a quartz tube with a diameter of one inch inside a tube furnace was cleaned with high-purity argon (Ar) gas for an hour. Then under a constant Ar gas flow rate (150 sccm), the furnace was rapidly heated to 850 °C. After that a quartz boat loaded with the CdS powders (99.995%) [mixed with $\sim$5% mass ratio of Cd (99.95%)] and the substrates was inserted into the quartz tube with the source at the upstream of the Ar gas. The distances between the source and the substrates were about 15–20 cm. The local temperatures for the source and the substrates were about 850 and 750 °C, respectively. The synthesis duration was about 45 minutes. Fig. 1b shows the field-emission scanning electron microscope (FESEM) images of the as-synthesized CdS NBs. We can see that on the same substrate (with a constant local temperature) the NBs are of uniform morphology. It is worth noting that some wire-like structures in this figure are the side faces of the NBs. The NBs are hundreds of microns in length, tens of nanometers in thickness, and around 1 μm in width. Significantly, by lowering the local temperature of the substrates to $\sim$720 °C, we can also synthesize CdS NWs with

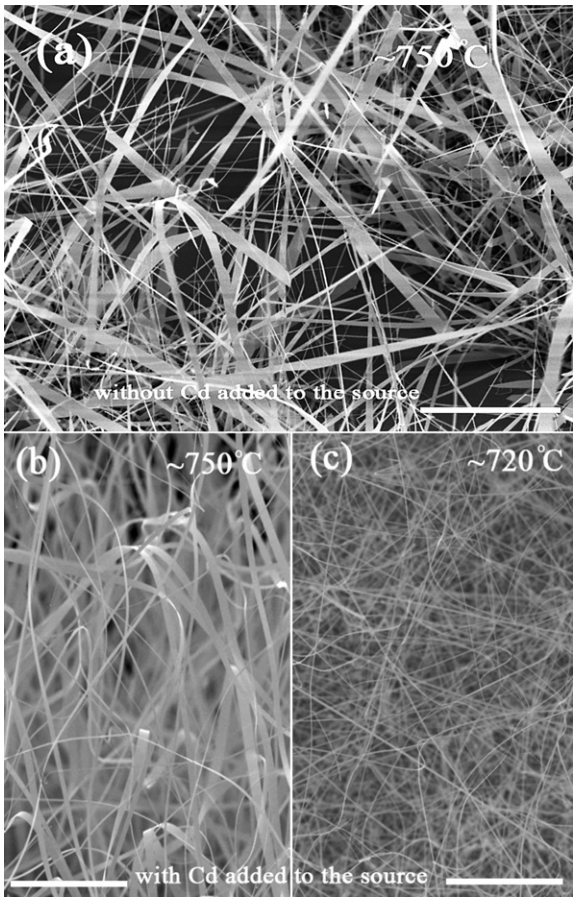

Fig. 1 FESEM images (scale bars: 10 μm) of CdS NBs synthesized *via* a common atmospheric VLS synthesis process (a) and *via* our improved VLS synthesis process (b) and (c). The corresponding substrate temperatures during the synthesis processes are shown in the figures.

uniform diameters of about 160 nm, as shown in Fig. 1c. Both the NBs and NWs exhibit good *n*-type conductance. We think the sulfur vacancies and/or cadmium interstitials serve as the shallow donors in the CdS NBs/NWs.

The inverters were fabricated as follows: firstly, a CdS NB suspension was dropped on oxidized p^+-Si substrates each with a 600 nm thick SiO_2 film on the top. Secondly, UV lithography followed by thermal evaporation and lift-off process was used to fabricate three ohmic contact In/Au electrodes (20/100 nm) on an individual *n*-CdS NB. The space distances between the neighboring ohmic electrodes are 20 μm. Thirdly, a high-κ dielectrics HfO_2 film (20 nm) was deposited to clad the NB by the atomic layer deposition (ALD) method. Finally, two Au top gate electrodes (3 μm wide, 120 nm thick) were made across the HfO_2/NB in between the In/Au electrodes by a similar process to that mentioned above. Fig. 2a and 2b are schematic illustrations of the fabrication process. The gray short lines show the way the circuit is connected. In our CdS NB inverter, two identical MISFETs formed between any neighboring ohmic contact electrodes are employed. One MISFET works as the driver (Q_D), the other works as the load (Q_L). Room-temperature (300 K) electrical transport measurements on the CdS NB devices were done with a semiconductor characterization system (Keithley 4200) in darkness.

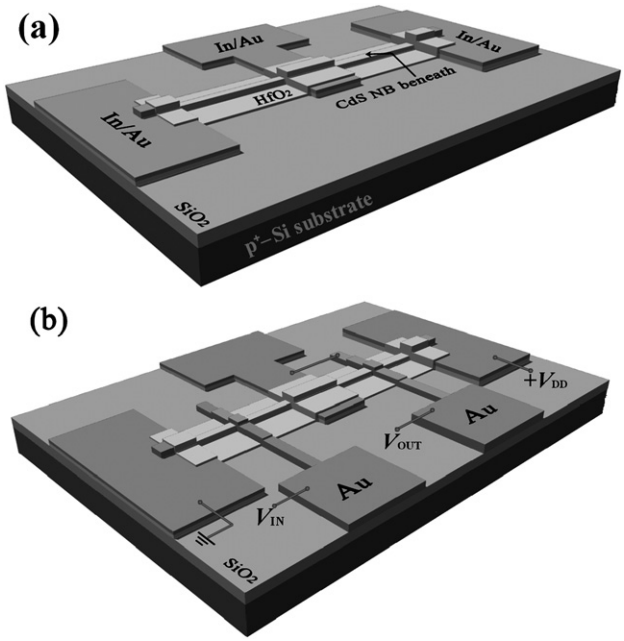

Fig. 2 Schematic illustrations for the inverter fabrication process. (a) Firstly, three ohmic contact electrodes with space distance of ~20 μm were fabricated on a CdS NB lying on a SiO_2/p^+-Si substrate. Then a 20 nm thick HfO_2 film was deposited by the ALD method; (b) Finally, two Au top gate electrodes (3 μm wide, 120 nm thick) were made across the HfO_2/NB in between the ohmic contact electrodes. The gray short lines show how the circuit is connected.

Results and discussion

Fig. 3a exhibits source-drain current (I_{DS}) and source-drain voltage (V_{DS}) relations measured at different gate voltages (V_{GS}) of a representative MISFET involved in the CdS NB inverter. During the measurement, the sources were grounded. Given a constant V_{GS}, I_{DS} increases linearly with V_{DS} at lower V_{DS} and saturates at higher V_{DS}. The channel conductance shows a drastic increase with the increase of applied positive V_{GS}, which indicates the MISFET is of *n*-channel. The inset highlights the I_{DS}-V_{DS} curve at $V_{GS} = 0$ V. This curve will be referenced in the discussion below. Fig. 3b is the gate transfer characteristic ($V_{DS} = 1$ V) with V_{GS} sweeping from −1 to +1 V. A high on/off ratio of about 8×10^7 is obtained. The threshold voltage V_{th} is very low ($\cong -0.1$ V), which will benefit the fabrication of low-power devices. Furthermore, the negative V_{th} for this *n*-channel MISFET indicates that it works in depletion mode (D-mode). The I_{DS} -V_{GS} relationship in the subthreshold region (the straight black line) gives a subthreshold swing *S* as small as 65 mV dec^{-1}, which is very close to the theoretical limit $S = (K_B T/q) \ln(10) = 60$ mV dec^{-1}.[22] *S* is a key parameter for transistors. Transistors with smaller *S* values tends to be switched on/off with greater speed, which is especially important for low V_{th} and low-power operation for FETs scaled down to a smaller size.[14,19,23] The inset of Fig. 3b is the I_{DS}-V_{GS} hysteresis curve on a linear scale, the arrows indicate the V_{GS} sweeping directions. We can see the hysteresis of the threshold voltage during the measurements is very small ($\Delta V_{th} \cong 30$ mV). A maximum transconductance value ($g_m = dI_{DS}/dV_{GS}$) of about 1.4 μ*S* can be

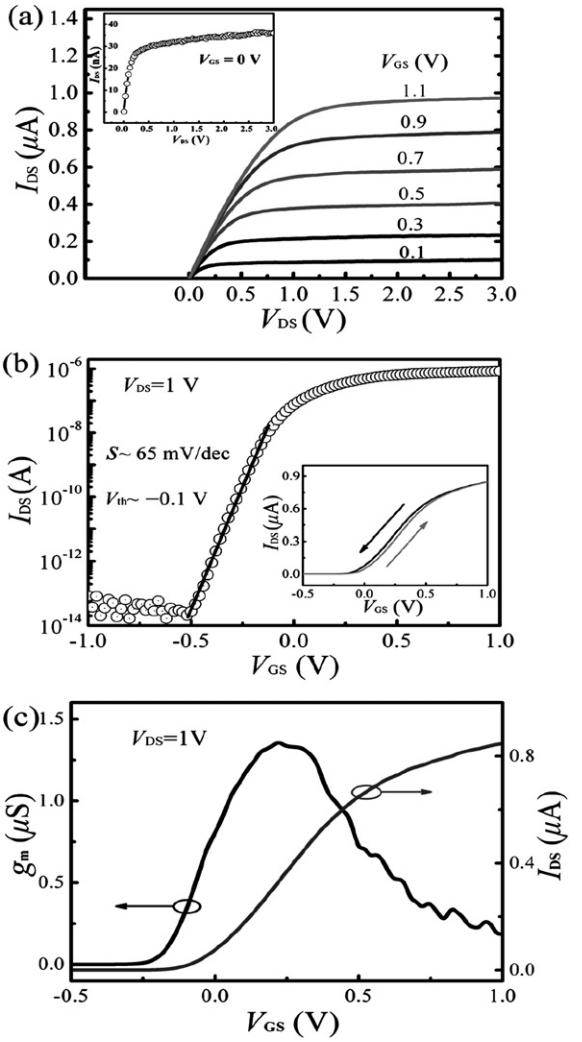

Fig. 3 The gate transfer characteristic of a representative CdS NB MISFET employed in the inverter. (a) Output characteristic family for this *n*-channel MISFET at various V_{GS}. The inset highlights the output characteristic at V_{GS} = 0 V; (b) I_{DS}-V_{GS} relation at V_{DS} = 1 V. The straight line highlights the subthreshold region. The inset exhibits the I_{DS}-V_{GS} hysteresis curve on a linear scale. (c) The g_m-V_{GS} (black) and the corresponding I_{DS}-V_{GS} (gray) curves.

obtained from the gate transfer characteristic curve (see Fig. 3c). The field-effect electron mobility (μ_e) of this MISFET can be estimated to be about 53 cm^2/(V s) using the equation $\mu_e = Lg_m/WC_0V_{DS}$,[25–27] where L is the channel length (20 μm), C_0 is the oxide capacitance per unit area ($= \varepsilon_r\varepsilon_0/d$), ε_r is the relative dielectrics constant of HfO_2 (~17), W is the gate width (equal to the width of NB in the FET, about 0.7 μm) and d is the thickness (20 nm) of the HfO_2 layer. The mobility values of our synthesized CdS NBs can be as high as ~300 cm^2/V s measured by fabricating CdS NB back-gate FETs,[24,25] which is close to the best reported value of bulk CdS single crystal materials (~340 cm^2/V s).[25] However, the field-effect mobility for our FETs had decreased to a much lower value as mentioned above when the surface of CdS NB was passivated by an HfO_2 film. Decrease of the mobility is commonly noticed in MISFETs with high-κ dielectrics, which is attributed to carrier scattering caused by the interface states between the high-κ dielectrics and the semiconductor conductive channel.[24,28] The reason that the CdS NB MISFETs with high-κ HfO_2 dielectrics as the top-gate insulator layer have good virtue, such as low threshold voltage, small subthreshold swing and hysteresis, has been discussed in detail in our previous work.[24]

Fig. 4a is the typical voltage transfer characteristic (VTC) of a CdS NB inverter with the V_{DD} set to be 5 V. The lower-left inset is a FESEM image of the inverter, the scale bar is 10 μm. The circuit diagram is shown next to the FESEM image. The gate voltage of the driver serves as the input (*i.e.*, $V_{GSD} = V_{IN}$). The gate and source of the load are connected, hence the gate voltage

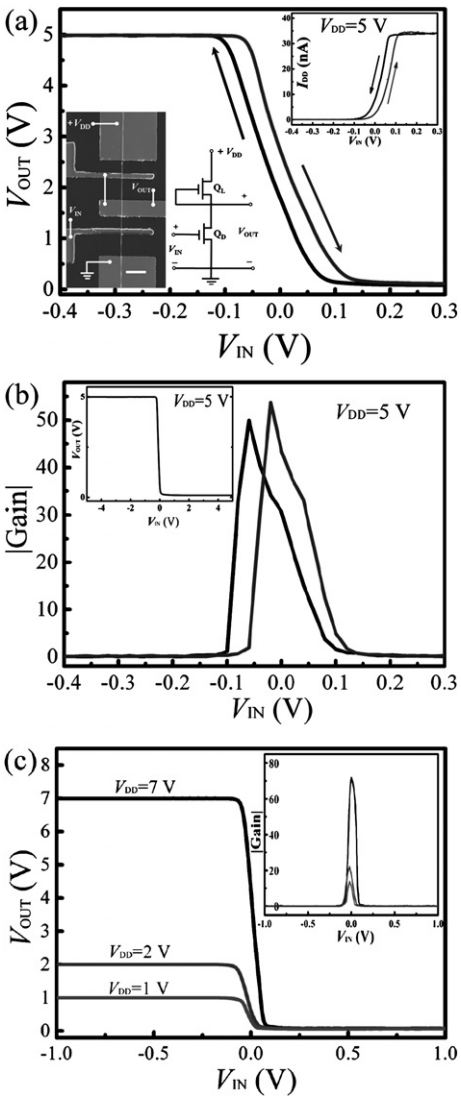

Fig. 4 (a) The VTC curves for an inverter operating at V_{DD} = 5 V. The arrows indicate the V_{IN} sweeping directions. The lower-left inset shows the FESEM image of the device (scale bar: 10 μm). A circuit diagram is next to it. The upper-right inset exhibits the corresponding current I_{DD} flowing through the inverter, the arrows indicate the V_{IN} sweeping directions; (b) voltage gain curves obtained from the corresponding VTC curves shown in Fig. 4a. The inset is the VTC for the inverter operating at V_{DD} = 5 V with V_{IN} sweeping from −5 to 5 V; (c) the VTC for the inverter under different supply voltage V_{DD}s. The inset gives the corresponding voltage gain curves.

of the load can always be taken as 0 V (*i.e.*, $V_{GSL} = 0$ V). The arrows indicate the V_{IN} sweeping directions. We can see clearly that the hysteresis, resulted from the hysteresis of the MISFETs involved in the inverter, is as small as about 30 mV. The upper-right inset exhibits the corresponding current flowing through the inverter (I_{DD}) during the measurement. We can see that I_{DD} increases with V_{IN} at lower value, and saturates at higher value (corresponding input is logic 1). The operating principle of the inverter can be understood as follows: when the V_{IN} is logic 0 (*e.g.*, $V_{IN} = -0.3$ V), the driver is cut off ($V_{th} \cong -0.1$ V), while the load transistor is at an on-state ($V_{GSL} = 0$ V). Hence, the current flowing through the inverter will be limited by the driver, and accordingly V_{OUT} is close to V_{DD} ($V_{OUT} = V_{DD} - V_{DSL}$) (logic 1). With V_{IN} increasing, the driver becomes turned on, resulting in an increasing I_{DD}. When the I_{DD} reaches the saturated current of the load ($I_{DSL(sat)} \cong 33$ nA as shown in the inset of Fig. 3a) (corresponding V_{IN} is logic 1), the load will enter its saturation region, and behaves like a big dynamic resistance ($dI_{DSL}/dV_{DSL} = 0$).[29] In this case, most supply voltage will drop on the load, and V_{OUT} is close to zero (logic 0).

For an inverter to work as a part of more complicated logic system, a voltage gain ($\beta = \Delta V_{OUT}/\Delta V_{IN}$) of at least 1 is required.[14,19] Fig. 4b shows the voltage gain curves obtained from the corresponding VTC curves shown in Fig. 4a. A maximum voltage gain of about 54 is obtained at $V_{DD} = 5$ V. Besides, superior to the inverter based on CdS NW MESFETs, the as-constructed inverters can work in a much larger input range with highly stable output voltages. The inset is the VTC for the inverter operating at $V_{DD} = 5$ V with V_{IN} sweeping from -5 to 5 V. We can see that the V_{OUT} value remains quite stable at either the logic 1 or logic 0 state. Fig. 4c displays the VTCs of the inverter under different supply voltages. It is clear that the high and low output voltages (V_{OH} and V_{OL}) are very close to the supply voltage and zero, respectively. This characteristic is a good virtue as it can make full use of the supply voltage and yield a very small low output voltage.[30] The inset of Fig. 4c shows the corresponding voltage gain curves for the inverter operating at 1, 2 and 7 V are about 14, 22 and 72, respectively. The voltage gain 72 is the highest value reported for the inverter based on NB/NW *n*-channel MISFETs so far. Besides, the fact that the inverter can work at a supply voltage low to 1V with a voltage gain high to 14 means that the inverter can be used as low-power device in the future. We think the high performance of the inverter is a direct result of the low threshold voltage and high channel conductance of the CdS NB MISFETs employed.

Encouraged by the desirable performances of the CdS NB devices presented above, we moved on to construct NAND and NOR logic gates, by introducing another similar CdS NB MISFET fabricated on another oxidized Si substrate. Their electrodes were rationally interconnected *via* aluminium wires. The circuit diagram and the characteristic of a NAND logic gate are shown in Fig. 5a. The input logic 0 and 1 are set as -0.3 and 0.3 V, respectively. Only when V_{IN1} and V_{IN2} are both logic 1, the V_{OUT} is logic 0, otherwise the V_{OUT} is logic 1. The logic relation $V_{OUT} = \overline{V_{IN1} \cdot V_{IN2}}$ indicates this device is a NAND logic gate. Fig. 5b exhibits the corresponding results of a NOR gate ($V_{OUT} = \overline{V_{IN1} + V_{IN2}}$). The circuit diagram is also shown in this figure. Only when both of the inputs are logic 0, *i.e.* both of the drivers are switched off, the V_{OUT} is logic 1. Otherwise the V_{OUT} is logic 0. We have fabricated more than 20 such inverters, NAND and NOR gates. Most of them exhibit similar characteristics.

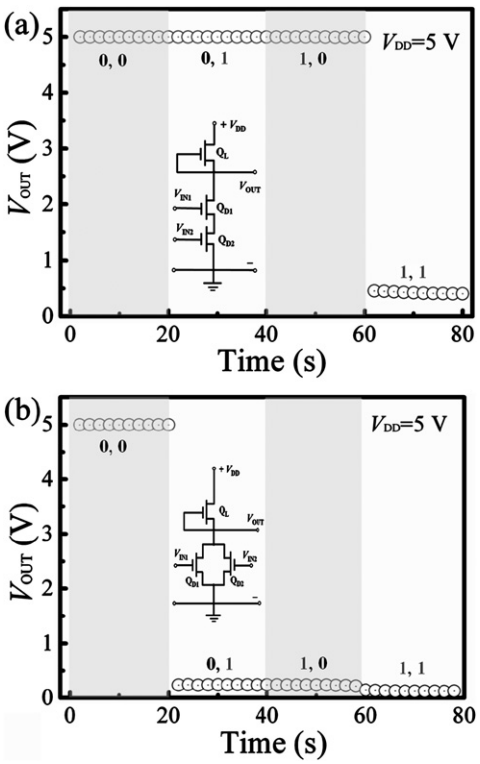

Fig. 5 (a) Output voltage of a NAND gate for four possible input states: (0, 0), (0, 1), (1, 0), (1, 1). The logic relation $V_{OUT} = \overline{V_{IN1} \cdot V_{IN2}}$ is revealed. (b) Output voltage of a NOR gate for the four possible input states. The logic relation $V_{OUT} = \overline{V_{IN1} + V_{IN2}}$ is revealed. Corresponding circuit diagrams are plotted in respective figures. Here, the logic input 0 is -0.3 V, and the logic input 1 is 0.3 V.

Conclusion

In summary, we have obtained high-quality CdS NBs with uniform morphology, by adding a tiny Cd grain to the source in the VLS process. Based on these CdS NBs, high-performance logic gates, such as NOT (inverter), NAND and NOR gates, have been constructed. The Au/high-κ HfO_2/*n*-CdS NB MISFETs employed in these logic gates show excellent performances, such as low threshold voltage (~ -0.1 V), high on/off ratio ($\sim 10^8$), small subthreshold swing ($\sim$65 mV dec^{-1}) and voltage hysteresis ($\sim$30 mV). The peak voltage gain of the inverter is as high as 72 ($V_{DD} = 7$ V), which is the best result reported, as far as we know, for inverters made on NB/NW *n*-channel MISFETs. Besides, the inverters have some more merits,[30] such as: they can work in a larger input range with highly stable output voltages, and can work at low supply voltages. Their high output voltages can make full use of the supply voltages, and their output low voltages can be close to zero. These results demonstrate that the Au/high-κ HfO_2/CdS NB MISFETs can be ideal building blocks for functional digital circuits.

Acknowledgements

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