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Electrical properties of Cu doped p-ZnTe nanowires

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Abstract
Single crystalline zincblende p-ZnTe nanowires (NWs) were synthesized via the vapour phase transport method. Based on either as-grown or Cu doped ZnTe NWs, single NW field effect transistors were fabricated and they were used to study the electrical properties of ZnTe NWs. Electrical transport measurements show that the as-grown ZnTe NWs are of p-type and very high resistivity. After 30 min immersion in $Cu(NO_3)_2$ solution, their conductivity can be increased by about three orders of magnitude. The hole concentrations of the p-type ZnTe nanowires could be controlled in a range from 7.0×10^{17} to 3.5×10^{18} cm^{-3} by changing the immersion duration. The doped p-type ZnTe NWs may have potential applications in nanoscale electronic and optoelectronic devices.

1. Introduction

Semiconductor nanowires (NWs), as fundamental building blocks for nanoscale electronic/photonic devices, have stimulated intensive research interest [1–9]. With research going deeper, finding effective ways to control doping at the nanoscale level becomes more and more urgent, because unintentionally doped semiconductor NWs usually have high resistivities [4, 6], which will limit their performance in both electronic and optoelectronic devices. ZnTe is a group II–VI semiconductor material with a direct band gap of 2.26 eV at 300 K. It has potential applications in optoelectronic devices, such as green light-emitting diodes, electro-optic detectors, and solar cells etc [10, 11]. To date, various methods have been used to synthesize ZnTe nanowires/nanorods [12–15]. Controlled doping of p-type or n-type bulk ZnTe or thin film ZnTe has been reported previously [16–19]. However, to the best of our knowledge, there have been no reports on the doping or the electrical transport measurements in ZnTe NWs. In this paper, we report controlled doping of p-type ZnTe NWs, and fabrication of ZnTe single NW field effect transistors (SNW-FETs) with these NWs.

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2. Experiments

The ZnTe nanowires were synthesized on Si substrates via a vapour phase transport method using ZnTe powders as the source, and Au as the catalyst. The experimental details have been described previously [13]. The morphology of the ZnTe nanowires was analysed using a field emission scanning electron microscope (FESEM) (Amray 1910 FE). The microstructure of the nanowires was characterized using a high-resolution transmission electron microscope (HRTEM) (Tecnai F30). The p-type doping of the ZnTe nanowires was carried out using a post-growth copper (Cu) doping method [18]. First, the as-grown ZnTe nanowires were dispersed in ethanol using an ultrasonic process. Then the ZnTe nanowire suspension was dropped on oxidized p-Si substrates (the SiO_2 layer is 600 nm). Later, the substrates with dispersed ZnTe NWs were immersed in a $Cu(NO_3)_2$ solution prepared by dissolving 0.1 g $Cu(NO_3)_2$ in 500 ml H_2O. Various durations, from 10 min to 24 h, were tested. Finally, the substrates were removed, adequately rinsed with de-ionized water, and placed in a vacuum-sealed quartz tube placed inside a horizontal tube furnace for annealing. The annealing temperature and duration were 400 °C and 1 h,

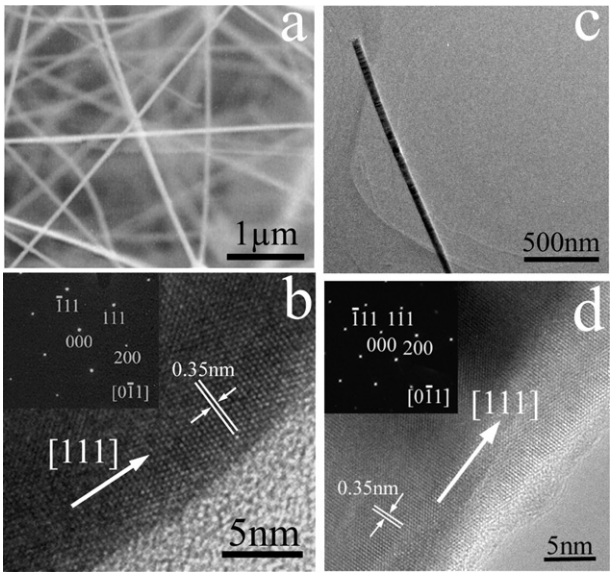

Figure 1. (a) A FESEM image of as-grown ZnTe nanowires. (b) A HRTEM image of an as-grown ZnTe nanowire. The arrow highlights the growth direction. The inset shows the corresponding SAED pattern recorded along the $[0\bar{1}1]$ zone axis. (c) and (d) The TEM and HRTEM images, respectively, of a Cu doped ZnTe nanowire, which indicate that the lattice structure of the Cu doped ZnTe nanowire is the same as that of the as-grown ZnTe nanowire.

respectively. This process aimed to activate the Cu dopants. Both the as-grown and the Cu doped ZnTe nanowires were fabricated into SNW-FETs on similar oxidized p-Si substrates mentioned above. The ohmic contacts to source and drain were fabricated by thermally evaporating Ni/Au (10 nm/120 nm) films on photoresist patterned by UV lithography, followed by a lift-off process. Here, high work function Ni was selected to reduce the contact barriers between ZnTe nanowires and the metal electrodes. The underlying p-Si substrate was used as the back gate by forming an ohmic contact with an Al electrode. The electrical transport measurements on the ZnTe SNW-FETs were conducted with a semiconductor parameters characterization system (Keithley 4200). For the electrical transport measurements of the ZnTe SNW-FETs, the source electrodes were grounded.

3. Results and discussion

Figure 1(a) shows a FESEM image of as-grown ZnTe nanowires, which are about 100 nm in diameter, and more than 10 μm in length. Figure 1(b) shows a HRTEM image of as-grown ZnTe nanowires, where the lattice planes are clearly seen with a spacing distance of about 0.35 nm along the growth direction. The inset of figure 1(b) is the corresponding selected area electron diffraction (SAED) pattern recorded along the $[0\bar{1}1]$ zone axis. The corresponding Miller indices are labelled. The HRTEM image together with the SAED pattern demonstrates that the ZnTe nanowires are single crystals with a cubic structure, and the growth direction is [111]. The TEM and HRTEM images of Cu doped ZnTe nanowires are shown in figures 1(c) and (d), respectively. The lattice structure of the Cu doped ZnTe nanowire is the same as that of the as-grown ZnTe nanowire.

Figures 2(a) and (b) show a schematic illustration and a FESEM image of a fabricated ZnTe SNW-FET. The channel length (L) of this FET is about 4 μm. Figure 2(c) shows the source–drain current (I_{ds}) versus voltage (V_{ds}) curves under various gate biases (V_g) for a SNW-FET made from an as-grown ZnTe nanowire. The I_{ds}–V_{ds} curves are symmetric but not linear, indicating a non-ohmic contact behaviour between the electrodes and the ZnTe NW. For identical V_{ds}, the I_{ds} decreases when V_g varies from −40 V to +20 V. This phenomenon suggests that the as-grown ZnTe nanowire is p-type. This is consistent with the well-known fact

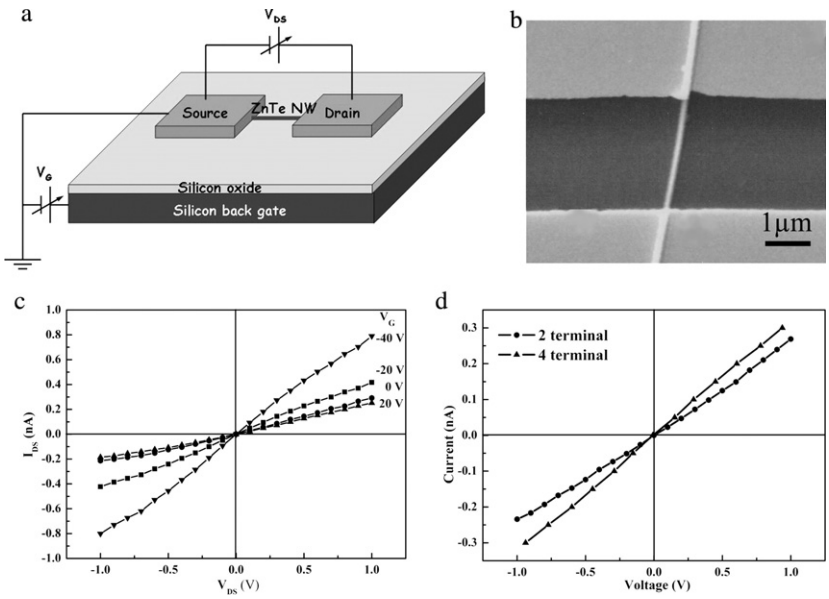

Figure 2. (a) Schematic illustration of a single ZnTe nanowire FET. (b) A FESEM image of a single ZnTe nanowire FET. (c) I_{ds}–V_{ds} characteristics of an as-grown ZnTe nanowire FET under gate bias ranging from −40 V to +20 V with a step of 20 V. (d) The I–V curves obtained from the two-terminal and the four-terminal measurements.

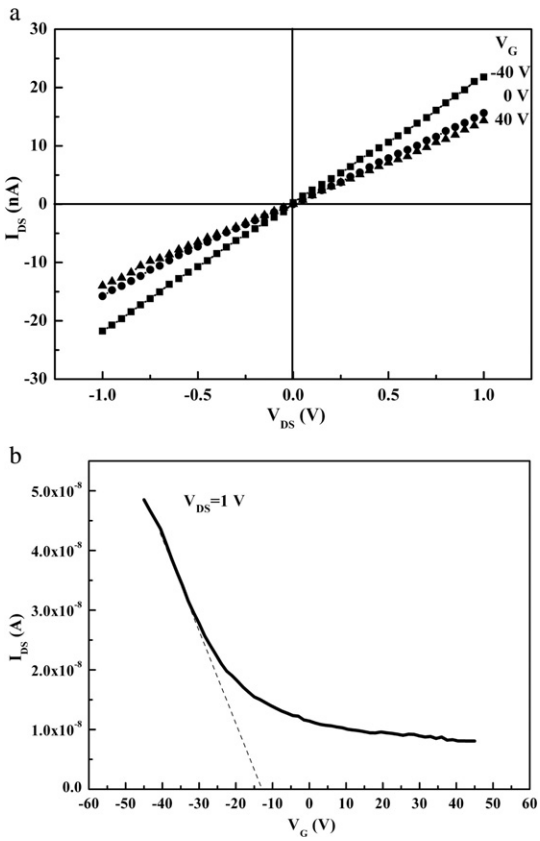

Figure 3. (a) I_{ds}–V_{ds} curves of a FET made of a ZnTe nanowire which had been immersed in Cu solution for 10 min under $V_g = -40, 0, +40$ V. (b) I_{ds}–V_g curves of the ZnTe nanowire FET at $V_{ds} = 1$ V. The threshold gate voltage (V_{th}) obtained by extrapolation from the linear region of the curve is −13 V.

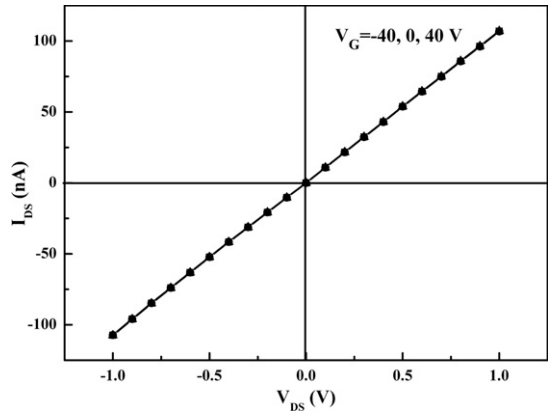

Figure 4. I_{ds}–V_{ds} characteristic of a FET made of a ZnTe nanowire which had been immersed in Cu solution for 30 min under $V_g = -40, 0, +40$ V.

that unintentionally doped ZnTe tends to exhibit a p-type characteristic [16, 17]. In order to estimate the resistivity of as-grown ZnTe nanowires, we conducted four-terminal measurements. The result is shown in figure 2(d). The measured resistance is about 3.1×10^9 Ω. Taking the dimensions of the nanowire (4 μm long, 100 nm thick) into account, we calculate the resistivity (ρ) of the as-grown ZnTe nanowire to be about 613.6 Ω cm. For comparison, the I–V curve between two terminals was also measured (figure 2(d)), which gives a resistance of about 3.7×10^9 Ω. Thus, the contact resistance between the electrodes and the as-grown ZnTe nanowire can be estimated to be about 0.6×10^9 Ω.

Figure 3(a) shows the I_{ds}–V_{ds} curves under $V_g = -40$, 0, +40 V for a SNW-FET made from a Cu doped ZnTe nanowire which had been immersed in the $Cu(NO_3)_2$ solution for 10 min. The I_{ds}–V_{ds} curves of this SNW-FET are linear and symmetric, indicating that the Ni/Au electrodes have formed good ohmic contacts with the Cu doped ZnTe nanowire. The resistivity of the ZnTe nanowire (4 μm long, 100 nm thick) is calculated to be about 12.5 Ω cm, much lower than that for the as-grown ZnTe nanowire. Figure 3(b) shows the I_{ds}–V_g curve measured at $V_{ds} = 1$ V. Again, the I_{ds} versus V_g relation shows that this ZnTe NW is p-type. From the linear region of the curve, the threshold gate voltage (V_{th}) and the transconductance ($g_m = dI_{ds}/dV_g$) can be extrapolated to be −13 V and 1.7 nS, respectively. The channel mobility of the device, μ_h, can be estimated to be about 1 $cm^2\ V^{-1}\ s^{-1}$ (comparable to the value of ZnTe thin films [19]), with the equation $\mu_h = g_m \frac{L^2}{CV_{ds}}$ [7], where C is the capacitance of the nanowire, and the L is the channel length of the SNW-FET. The nanowire capacitance C is given by $C = \frac{2\pi\varepsilon\varepsilon_0 L}{\ln(2h/r)}$ [7], where ε is the relative dielectric constant of SiO_2 (=3.9), h is the thickness of the silicon oxide layer, and r is the nanowire radius. The hole concentration (p) can be estimated to be about 7.0×10^{17} cm^{-3} from the equation $p = \frac{CV_{th}}{e\pi r^2 L}$ [7]. We also calculate the hole concentration from the equation $\rho = \frac{1}{pe\mu_h}$, which gives a p value of about 5.0×10^{17} cm^{-3}, very close to the value obtained previously. In order to further investigate the effectiveness of the doping process, we estimate the hole concentration of the as-grown ZnTe NW from the equation $\rho = \frac{1}{pe\mu_h}$. By using the above calculated μ_h (∼1 $cm^2\ V^{-1}\ s^{-1}$) and ρ (∼613.6 Ω cm) values, p is calculated to be about 1.0×10^{16} cm^{-3}. It is worth noting that, as the carrier mobility should increase as the carrier concentration decreases, the real p value for the as-grown ZnTe NWs should be smaller. All these phenomena demonstrate that Cu atoms, acting as acceptors, have been effectively doped into ZnTe nanowires.

Figure 4 shows the I_{ds}–V_{ds} curve for a SNW-FET made from a Cu doped ZnTe nanowire which had been immersed in the $Cu(NO_3)_2$ solution for 30 min. The excellent linear characteristic of the I_{ds}–V_{ds} curve indicates a good ohmic contact behaviour between the nanowire and the electrodes. The resistivity of the ZnTe nanowire is calculated to be about 1.8 Ω cm, about three orders of magnitude lower than that of the as-grown ZnTe nanowires. The hole concentration is estimated to be about 3.5×10^{18} cm^{-3} from the equation $\rho = \frac{1}{pe\mu_h}$, using the above calculated μ_h value (∼1 $cm^2\ V^{-1}\ s^{-1}$). The hole concentration here might be underestimated due to the overestimated μ_h value. The increased hole concentration results from the longer immersion duration. No field effect can be observed in this SNW-FET, indicating that the ZnTe NW here behaves like degenerately doped metallic nanowire [6, 20]. We find that the hole concentration in the ZnTe NWs no longer increases when the immersion duration exceeds 30 min. We think that this is because the doping level in a ZnTe NW is determined by the amount of Cu ions surrounding the surface of the ZnTe nanowire, and this amount of Cu ions may saturate when the immersion duration exceeds a certain value.

4. Conclusion

In conclusion, single crystalline zincblende p-ZnTe nanowires were synthesized via the vapour phase transport method. Effective post-growth doping of these nanowires was carried out by immersing them in the $Cu(NO_3)_2$ solution. The electrical characteristics of these ZnTe nanowires were investigated by fabricating them into SNW-FETs. The results show that the hole concentration of the p-type ZnTe nanowires could be controlled in a range from 7.0×10^{17} to 3.5×10^{18} cm^{-3} by controlling the immersion duration. For the Cu doped ZnTe NWs, a resistivity of about three orders of magnitude lower than that of as-grown ZnTe NWs was obtained.

Acknowledgments

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