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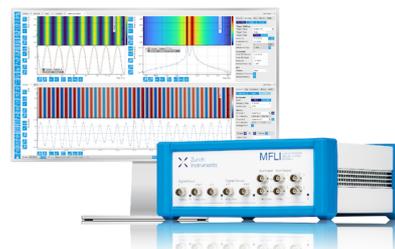Optoelectronic characteristics of single CdS nanobelts

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Synthesis of high quality *n*-type CdS nanobelts and their applications in nanodevices

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High quality *n*-type CdS nanobelts (NBs) were synthesized via an *in situ* indium doping chemical vapor deposition method and fabricated into field effect transistors (FETs). The electron concentrations and mobilities of these CdS NBs are around $(1.0 \times 10^{16} - 3.0 \times 10^{17})/\text{cm}^3$ and $100 - 350 \text{ cm}^2/\text{V s}$, respectively. An on-off ratio greater than 10^8 and a subthreshold swing as small as 65 mV/decade are obtained at room temperature, which give the best performance of CdS nanowire/nanobelt FETs reported so far. *n*-type CdS NB/p^+-Si heterojunction light emitting diodes were fabricated. Their electroluminescence spectra are dominated by an intense sharp band-edge emission and free from deep-level defect emissions. © *2006 American Institute of Physics*. [DOI: 10.1063/1.2387982]

Semiconductor nanobelts (NBs), a prominent type of one dimensional nanostructures,[1] are good candidates of building blocks for functional nanodevices such as waveguides,[2,3] photoconductive optical switches,[4,5] sensors,[6] acoustic resonators,[7] and field effect transistors (FETs).[8] Up to now, various semiconductor NBs have been synthesized.[1,2,9–15] Among them, CdS NB is one of the most important nanomaterials,[3–5,13–17] due to its potential applications in nano-optoelectronics. However, unintentionally doped CdS NBs have high resistivities,[4,5] which will limit its performances in both electronic and optoelectronic devices. In this letter, high quality *n*-type CdS NBs have been synthesized via an *in situ* indium (In) doping chemical vapor deposition (CVD) method and have been fabricated into nanobelt field effect transistors (NB-FETs). Experiment results show that In atoms have been effectively doped into the CdS NBs as shallow donors. The as-fabricated NB-FETs have the best performances among the CdS nanowire/nanobelt FETs (NW/NB-FETs) reported so far. In addition, CdS NB/p^+-Si heterojunction light emitting diodes (LEDs) have been fabricated. Their electroluminescence (EL) properties have been studied. For comparison, unintentionally doped CdS NBs were also synthesized and investigated.

The In doped CdS NBs were synthesized via a CVD method. CdS (99.995%) powders were used as the source, and pieces of Si wafers covered with 10 nm thick thermally evaporated Au catalysts were used as the substrates. Small amount of In (6*N*) grain was used as the doping source. Prior to heating, a quartz tube inside a tube furnace was cleaned with high-purity argon (Ar) for 90 min. Then under a constant Ar flow [200 SCCM (SCCM denotes cubic centimeter per minute at STP)], the furnace was rapidly heated to 850 °C. A quartz boat loaded with In grain, CdS powders,

and Si substrates in sequence was inserted into the quartz tube, with In grain at the upstream side of the flowing Ar. The distance between In and CdS was about 20 cm, and that between CdS and the Si substrates was about 10 cm. The synthesis duration was about 2 h. The unintentionally doped CdS NBs were synthesized under similar experimental conditions except for using the In doping source. The synthesized products were characterized by using field emission scanning electron microscope (FESEM) (AMRAY 1910 FE) and high-resolution transmission electron microscope (HR-TEM) (Tecnai F30) equipped with an energy-dispersive x-ray (EDX) spectroscope. Room temperature electrical transport measurements on CdS NB-FETs were done with a semiconductor characterization system (Keithley 4200). The EL measurements of the CdS NB/p^+-Si heterojunction LEDs were done with a microzone confocal Raman spectroscopy (HORIBA Jobin Yvon, LabRam HR 800) equipped with a color charge-coupled device (CCD) camera.

The FESEM and HRTEM results of In doped and unintentionally doped CdS NBs are similar. Figure 1(a) shows a typical FESEM image of such CdS NBs. We can see that the CdS NBs have smooth surfaces and uniform widths along the growth directions. Usually, the CdS NBs are about sev-
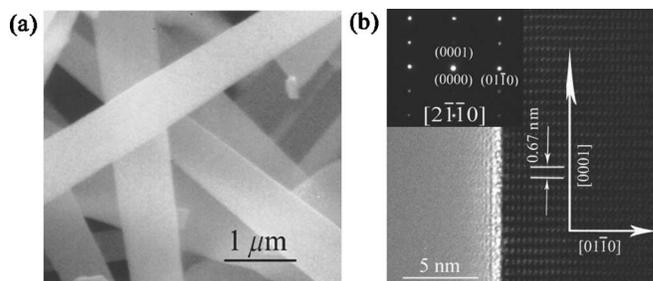

FIG. 1. (a) Typical FESEM image of CdS NBs. (b) HRTEM image of a CdS NB; the inset is the corresponding SAED pattern recorded along the $[2\bar{1}\bar{1}0]$ zone axis.

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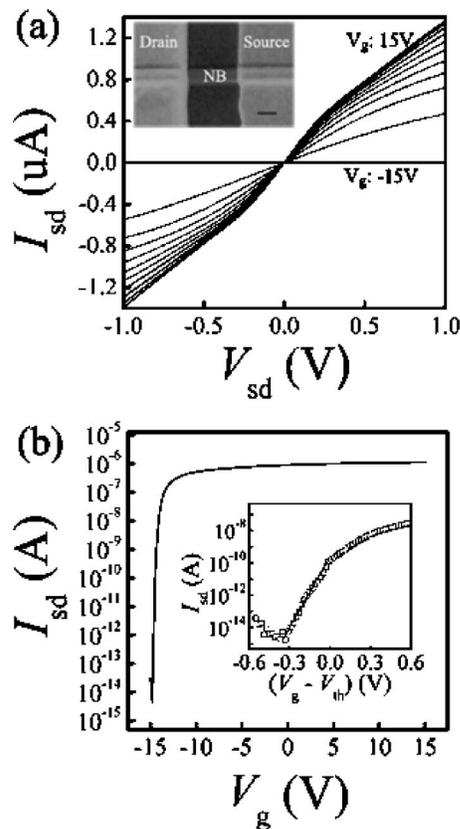b)Author to whom correspondence should be addressed; electronic mail: lundai@pku.edu.cn

FIG. 2. (a) I_{sd}-V_{sd} curves with V_g from -15 to 15 V, in steps of 3 V. Inset: A FESEM image of an In doped CdS NB-FET. The scale bar is 1 μm. (b) The log I_{sd}-V_g curve ($V_{sd}=0.8$ V). Inset: Magnified I_{sd} vs V_g relation at the subthreshold region.

eral hundred microns in length, $0.3-10$ μm in width, and $50-300$ nm in thickness, which can be partially controlled by the synthesis temperature. Figure 1(b) is a HRTEM image of a CdS NB. The corresponding selected area electron diffraction (SAED) pattern recorded along the $[2\bar{1}\bar{1}0]$ zone axis is shown in the inset. The lattice planes with space distance of about 0.67 nm are clearly seen along the growth direction. According to JCPDS data,[18] these planes can be indexed as (0001) planes. Corresponding Miller indices are labeled in the SAED pattern. The HRTEM measurements demonstrate that the synthesized NB is single crystal wurtzite CdS, and the growth direction is [0001]. No In element is detected in the In doped CdS NBs by the EDX spectroscope with a sensitivity of 1%.

The CdS NB-FETs were prepared by dropping CdS NBs suspension onto oxidized p-Si ($\sim$10 Ω cm) substrates which have a SiO$_2$ layer of about 600 nm thick. UV lithography and lift-off processes were used to define the source and drain In/Au electrodes. The underlying p-Si was used as back gate. Field effect is barely observed in the NB-FETs fabricated with the unintentionally doped CdS NBs which have a resistivity around 10^4 Ω cm. The inset of Fig. 2(a) shows FESEM image of a CdS NB-FET fabricated with an In doped CdS NB. The width W and thickness T of the CdS NB are about 780 and 200 nm, respectively. The spacing L between the source and drain electrodes is about 2.6 μm. Figure 2(a) shows the source-drain current (I_{sd}) versus source-drain voltage (V_{sd}) relations measured at various gate voltages (V_g) from -15 to $+15$ V. It clearly shows that the device is n-type depletion-mode FET. From I_{sd}-V_{sd} curve

measured at $V_g=0$, and dimensions of the CdS NB, we can obtain the resistivity (ρ) of the CdS NB to be about 3.72 Ω cm, much lower than that of the unintentionally doped CdS NBs. This indicates that the electron concentration in the In doped CdS NBs has increased dramatically. The I_{sd} vs V_g relation ($V_{sd}=0.8$ V) on an exponential scale is shown in Fig. 2(b). From this curve, a threshold voltage V_{th} is read to be -13.5 V, and an on-off ratio is obtained to be greater than 10^8. This is the largest on-off ratio reported for CdS NW/NB-FETs so far.

From the magnified I_{sd} vs V_g relation at the subthreshold region shown in the inset of Fig. 2(b), we obtain a subthreshold swing of about 65 mV/decade, which is quite close to the theoretical limit value of 60 mV/decade.[19] The carrier concentration (n_e) and the electron mobility (μ_e) can be estimated by $n_e=C_GV_{th}/eWLT$ or $n_e=1/\rho q \mu_e$ and $\mu_e=g_m(L^2/C_GV_{sd})$, where C_G is the gate capacitance and $g_m(=dI_{sd}/dV_g)$ is the transconductance.[19,20] The g_m value is obtained to be about 200 nA/V at $V_{sd}=0.8$ V. Assuming a parallel plate capacitor model in our CdS NB-FETs, $C_G=\varepsilon\varepsilon_0 LW/h$, where ε and h are the relative dielectric constant and thickness of SiO$_2$,[8] we deduce $n_e\approx 2.4\times 10^{16}$ cm^{-3} and $\mu_e\approx 146$ cm^2/V s. Measurements on more than ten CdS NB-FETs give a distribution of electron concentrations and electron mobilities of around $(1.0\times 10^{16}-3.0\times 10^{17})$/cm^3 and $100-350$ cm^2/V s, respectively. These mobilities are comparable to those of bulk CdS single crystal materials ($\sim$340 cm^2/V s). These results indicate that the In atoms have been effectively doped into the CdS NBs as shallow donors, and the In doped n-type CdS NBs are with high electrical quality.

The CdS NB/p^+-Si heterojunction LEDs were fabricated as follows: First, p^+-Si pads (200 μm long, 50 μm wide) were patterned by UV lithography followed by inductively coupled plasma etching on silicon-on-insulator (SOI) substrates with a 100 nm thick SOI and a 380 nm thick box. Then CdS NBs were assembled across the edges of the Si pads to form nanoheterojunctions. In/Au electrodes to CdS NBs were defined the same way as that mentioned above. The FESEM image of an as-fabricated device is shown in the inset of Fig. 3(a). No light emissions could be observed in the unintentionally doped CdS NB/p^+-Si heterojunctions due to the very low injected current density.

A typical I-V curve of an In doped n-CdS NB/p^+-Si heterojunction LEDs is shown in Fig. 3(a). A good rectification characteristic is present. The turn-on voltage is around 1.7 V. When the forward bias is above 5 V, green light spots can be seen from the LEDs even by naked eyes. The inset of Fig. 3(b) shows a room temperature EL image of a LED at a forward bias of 8 V recorded by a color CCD camera. Figure 3(b) shows the EL spectrum measured at light spot. We can see an intense sharp CdS band-edge emission peaked around 506 nm with full width at half maximum of only about 11 nm. The well known deep-level defect emissions from CdS, which may be due to radiative recombination involving impurity and/or defect levels,[21] have not been found in this spectrum. These results indicate the In doped n-type CdS NBs are with high crystal quality.

In conclusion, high quality n-type CdS NBs have been synthesized via an *in situ* In doping CVD method and have been fabricated into CdS NB-FETs and CdS NB/p^+-Si heterojunction LEDs. The mobilities of these CdS NBs are com-
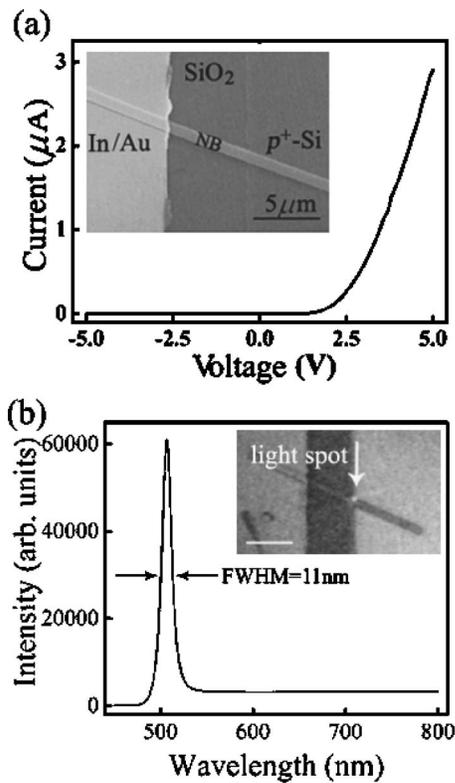
FIG. 3. (a) Typical *I-V* curve of an In doped *n*-CdS NB/p^+-Si heterojunction LED. Inset: FESEM image of an In doped *n*-CdS NB/p^+-Si heterojunction LED. (b) Room temperature EL spectrum measured at a light spot. Inset: EL image recorded at a forward bias of 8 V. The scale bar is 5 μm.

parable to those of bulk CdS single crystal materials. The *n*-type CdS NB-FETs have the largest on-off ratio and the smallest subthreshold swing reported for CdS NW/NB FETs so far. The EL spectra of the *n*-type CdS NB/p^+-Si heterojunction LEDs are dominated by intense sharp band-edge emission and free from deep-level defect emissions. The high performances of these nanodevices indicate that the In doped CdS NBs may have wide potential applications in the future.

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